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ThinkPad 600
Technical Reference

Note

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First Edition (April 1998)

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Preface

This technical reference contains hardware and software interface information specific to the IBM ThinkPad 600 computer. This technical reference is intended for those who develop hardware and software products for the computer. Users should understand computer architecture and programming concepts.

This publication consists of the following sections and appendixes:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "System Board," describes the system-specific hardware implementations.

Section 3, "Subsystems," describes the hardware functions specific to the ThinkPad 600 computer.

Appendix A, "System Resources," describes the available system resources for the computer and docking stations.

Appendix B, "System Management API (SMAPI) BIOS Overview," describes the system software interface built into the system, called the System Management Application Program Interface (SMAPI) BIOS, which controls the system information, system configuration, and power management features of the ThinkPad computer.

Appendix C, "Appendix C," contains special notices and trademark information.

An index is also included.

Attention

The term *Reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. Read the register first and change only the bits that must be changed.

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Description

The IBM ThinkPad 600 computer (hereafter called the *ThinkPad computer* or the *computer*) is a notebook-size computer that features AT bus architecture. Each computer supports one UltraSlim Bay and one internal hard disk drive. The ThinkPad 600 computer also supports an internal CD-ROM drive or a diskette drive in the UltraSlim Bay.

Programs can distinguish the foregoing computer model from other ThinkPad models by reading the system ID:

Interrupt 15H

Function code (AH)=C0H.

Returns

ES:(BX+2) : Model Byte

ES:(BX+3) : Submodel Byte

The system microprocessor contains an internal cache and a cache controller.

Figure 1-1 lists the model bytes, submodel bytes, and system clock speed of the system board for each model.

Model	Model Byte (Hex)	Submodel Byte (Hex)	System Clock
600	FC	01	33 MHz

Figure 1-1. Model and Submodel Bytes

For a listing of the other systems, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface*.

System Board Devices and Features

Figure 1-2 lists the system board devices and their features. The *IBM Personal System/2 Hardware Interface Technical Reference* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	–	Intel Pentium processor with the MMX technology 233 MHz or Intel Pentium II processor 233 or 266 MHz
External cache	–	512 KB (write back)
System timers	1	Channel 0: system timer Channel 1: refresh generation Channel 2: tone generator for speaker
ROM subsystem	–	128 KB by 4 banks (1 KB equals 1024 bytes)
RAM subsystem	–	32 to 160 MB (1 MB equals 1,048,576 bytes)
CMOS RAM subsystem	–	128 bytes CMOS RAM with real-time clock/calendar + 4 KB NVRAM
EEPROM subsystem	–	1 K bits
Video subsystem	–	XGA video functions: Up to 65,536 colors on the TFT XGA (1024x768) LCD and HPA XGA (1024 x 768). Up to 16,777,216 colors on an external monitor See "Video Subsystem" on page 3-2 for more details on the video subsystem.
DMA controller	1	Seven DMA channels (AT compatible): Four 8-bit channels and three 16-bit channels

Figure 1-2 (Part 1 of 2). System Board Devices and Features

Device	Type	Features
Interrupt controller	1	15 levels of system interrupts (interrupts are edge-triggered)
Keyboard/auxiliary device controller	1	Internal keyboard TrackPoint Auxiliary device connector Password security
Diskette drive controller	2	Supports: 3.5-in. diskette (1.44 MB) 3.5-in. diskette (1.2 MB) 3.5-in. diskette (720 KB)
Serial controller port	2	EIA-232-E interface (16550 compatible) Programmable as serial port 1, 2, 3, or 4 One 9-pin, D-sub connector
Parallel controller port	1	Programmable as parallel port 1, 2, or 3 IEEE P1284-A compatible Supports bidirectional input and output Enhanced Parallel Port (EPP) compatible Extended Capabilities Port (ECP) compatible
Expansion bus adapter (PCI-bus)	–	Supports externally attached devices: SelectaDock docking system Port replicator
PCMCIA slots	–	Conforms to the standards for: CardBus Two Type I or II PC cards One Type III PC card
Modem subsystem	–	Is driven by: MDSP 3780i SRAM 32 Kb by 40 bits Crystal Audio Voice band CODEC for modem Internal DAA Internal omnidirectional microphone
Infrared subsystem	–	Supports: ThinkPad IR/SIR/D-ASK (500 KHz) IR
Universal serial bus (USB)	–	Supports: USB input and output devices Personal Computer Memory Card International Association

Figure 1-2 (Part 2 of 2). System Board Devices and Features

System Board I/O Address Map

Figure 1-3 is the I/O address map.

Address (Hex)	Device
0000–001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0022–002F	Reserved
0040–0043	System Timer 1
0048–004B	Reserved
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0062, 0066	Slave Controller
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0072, 0073	Extended RT and CMOS
0074, 0075, 0076	Reserved
0081–0083, 0087	DMA Page Registers (0–3)
0089–008B, 008F	DMA Page Registers (4–7)
0092	System Control Port A
0096	Reserved
0098	System Flash ROM Control Register (DCR 2282)
00A0, 00A1	Interrupt Controller (Slave)
00B2–00B3	Power Management Register
00C0–00DF	DMA Controller (4–7)
00F0–00FF	Reserved
0130–013F	ThinkPad Modem
0170–0177	Secondary IDE Registers
01F0–01F7	Primary IDE Registers
0201	Joystick Port
0220–0233	Audio Subsystem - Sound Blaster
0240–0253	Audio Subsystem - Sound Blaster
026E, 026F	Super I/O Configuration Registers
0260–0273	Audio Subsystem - Sound Blaster
0278–027A	Parallel Port 3
027B–027F	Reserved
0280–0283	Audio Subsystem - Sound Blaster
02E8–02EF	Serial Port 4
02E8–02EF	IR Port 4
02F8–02FF	Serial Port 2
02F8–02FF	IR Port 2
0300–0303	MIDI Port 1
0310–0313	MIDI Port 2
0320–0323	MIDI Port 3

Figure 1-3 (Part 1 of 2). System Board I/O Address Map

Address (Hex)	Device
0330–0333	MIDI Port 4
0350–035F	ThinkPad Modem
0376, 0377	Secondary IDE Registers
0378–037A	Parallel Port 2
037B–037F	Reserved
0388–038B	Audio Subsystem - FM Synthesizer
0398–0399	Reserved
03B4, 03B5, 03BA	Video Subsystem
03BC–03BE	Parallel Port 1
03C0–03C5	Video Subsystem
03C6–03C9	Video DAC
03CA, 03CC, 03CE, 03CF, 03D4, 03D5, 03DA, 03D8–03DA	Video Subsystem
03E0–03E1	PCMCIA Interface (DCR 2959)
03E8–03EF	Serial Port 3
03E8–03EF	IR Port 3
03F0–03F5, 03F7	Diskette-Drive Controller
03F6, 03F7	Primary IDE Registers
03F8–03FF	Serial Port 1
03F8–03FF	IR Port 1
0530–0537	Audio - WSS 1
0538–053F	Audio Control Port 1
0604–060B	Audio - WSS 2
0770–077F	ThinkPad Modem
0CF8–0CFB	PCI Configuration Address Register
0CFC–0CFF	PCI Configuration Data Register
0DB0–0DBF	ThinkPad Modem
0D38–0D3F	Audio Control Port 2
0E80–0E87	Audio - WSS 3
0E88–0E8F	Audio Control Port 3
0F40–0F47	Audio - WSS 4
0FF0–0FF7	Audio Control Port 4
15E8–15EF	Power Management Register
2120–21FF	Reserved
23C0–23C7	Reserved
EF00–EF37	Power Management Register
EFA0–EFAD	SMBus IO Space Register
F104	Reserved

Figure 1-3 (Part 2 of 2). System Board I/O Address Map

Specifications

Figure 1-4 to Figure 1-7 list the specifications for the computers.

Performance Specifications

Device/Cycle	Clock Counts (66 MHz)
Microprocessor	233 or 266 MHz
L1 cache (64bit) read/write hit	1 CPUCLK
L2 cache (64bit) (for not all models)	3-1-1-1(1-1-1-1)
read hit (back-to-back)	
write hit (back-to-back)	
Memory (64bit) (see Note)	
read, page hit	5-1-1-1
read, bank miss	8-1-1-1
read, page miss	11-1-1-1
posted write	3-1-1-1
write retire rate from write buffer	-1-1-1
Note: The cycle times shown for access to system board RAM are based on 66 MHz memory bus (SDRAM, CAS LATENCY=2)	

Figure 1-4. Performance Specifications

Physical Specifications

Size	Width: 300.0 mm (12 in.) Depth: 240.0 / 254.0 mm (9.6 / 10.16 in.) Height: 36.5 mm (1.46 in.)
Weight by model (approximate value)	21U 5.45 lb 31U 5.04 lb 41U 5.47 lb 51U 5.55 lb 61U 5.06 lb
Air Temperature	System on (without diskette) 5.0°C to 35.0°C (41°F to 95°F) System on (with diskette) 10.0°C to 35.0°C (50°F to 95°F) System off 5.0°C to 43.0°C (41°F to 110°F)
Humidity	System (without diskette) 8% to 95% System (with diskette) 8% to 80%
Maximum altitude	: 3,048 m (10,000 ft) in unpressurized conditions
Heat output:	56 W
Acoustical readings	(see Figure 1-7 on page 1-9)
Electrical	(see Figure 1-6 on page 1-9)
Electromagnetic compatibility:	FCC class B With battery pack installed. This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

Figure 1-5. Physical Specifications

Electrical Specifications

	(56 W)
Input voltage (V ac)	100–240
Frequency (Hz)	50/60
Input (kVA)	0.13
Range is automatically selected; sine wave input is required. At maximum configuration.	

Figure 1-6. Electrical Specifications

Acoustical Readings

	L_{WAd} in bels		L_{pAm} in dB		<L_{pA}>_m in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
600	4.40	3.90	35.0	30.0	30.0	25.5
600 (with SelectaDock III)	4.60	4.30	37.5	34.0	31.0	28.0
Notes:						
L _{WAd}	Is the declared sound power level for the random sample of machines.					
L _{pAm}	Is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.					
<L _{pA} > _m	Is the mean value of the A-weighted sound pressure levels at the 1 meter position for the random sample of machines.					
Operate	Shows the value while using the hard disk drive.					
All measurements made in accordance with ANSI S12.10 and reported in conformance with ISO 9296.						

Figure 1-7. Acoustical Readings

Power Supply

The power supply converts the ac voltage to dc voltage and provides power for the following:

- System board set
- Diskette drive
- Hard disk drive
- CD-ROM drive
- Auxiliary devices
- Keyboard
- LCD panel
- PCMCIA cards

Voltages

The power supply generates six different dc voltages: VCC5M, VCC3M, VCC12, and VCCSW. Figure 1-8 shows the maximum current for each voltage.

Output	Voltage (V dc)	Current (A)
VCC5M	+5.0	5.0
VCC3M	+3.3	5.0
VCC12	+12.0	0.50
VCCSW	+5.0	0.006

Figure 1-8. Power Supply Maximum Current

Output Protection

A short circuit placed on any dc output (between two outputs or between an output and a dc return) latches all dc outputs into a shutdown state, with no hazardous condition to the power supply.

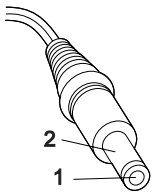
If an overvoltage fault occurs in the power supply, the power supply latches all dc outputs into a shutdown state before any output exceeds 135% of the nominal value of the power supply.

Voltage Sequencing

When power is turned on, the output voltages reach their operational voltages within 2 seconds.

Power Supply Connector

The following connector is used with the AC Adapter. The total power capacity of this connector must not exceed 4.0 A.



Refer to Figure 1-9 for the appropriate adapter pin assignments.

Pin	Voltage
1	+7.0 V dc to +17.0 V dc (depending on charging conditions)
2	Ground

Figure 1-9. Voltage Pin Assignments for the 56W AC Adapter

Battery Pack

The ThinkPad computer uses a lithium-ion (Li-ion) battery pack that meets the following electrical specifications:

Nominal Voltage	+10.8 V dc
Capacity (average)	3.2 ampere hours (AH)
Protection	Overcurrent protection Overvoltage protection Overdischarge protection Thermal protection

Figure 1-10. Lithium-Ion Battery Pack Specifications

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Description

This section describes the microprocessor, connectors, memory subsystems, and miscellaneous system functions and ports for the ThinkPad 600 computer.

Microprocessor

The ThinkPad 600 uses the Intel Pentium II 233 MHz processor with MMX technology or the Intel Pentium 233 or 266 MHz processor.

The processor has a 32-bit address bus and a 64-bit data bus. It is software-compatible with all previous microprocessors. The processor has an internal, split data and instruction, 32-KB write-back cache. It includes pipelined math coprocessor functions and superscalar architecture (two execution units).

Cache Memory Operation

In addition to the 32 KB of internal Level 1 (L1) cache memory in the microprocessor, the system board of the ThinkPad 600 computer contains an additional 512 KB of external Level 2 (L2) cache memory.

The cache memory in the Intel Pentium II microprocessor and the L2 external cache memory enable the microprocessor to read instructions and data much faster than if the microprocessor had to access system memory. When an instruction is first used or data is first read or written, it is transferred to the cache memory from main memory. This enables future accesses to the instructions or data to occur much faster.

The cache is disabled and empty when the microprocessor comes out of the reset state. The cache is tested and enabled during the power-on self-test (POST).

The cache memory in the Intel Pentium II microprocessor is loaded from system memory in 32-byte increments, each referred to as a *cache line*. A cache line is aligned on a paragraph boundary. A reference to any byte contained in a cache line results in the entire line being read into the cache memory (if the data was not already in the cache). When the microprocessor gives up control of the system

bus, the cache memory enters “snoop” mode and monitors all write and read operations. If memory data is written to a location in the cache and the cache line is in the “modified” state, the corresponding cache line is written back to system memory and invalidated.

When the microprocessor performs a memory read, the data address is used to find the data in the cache. If the data is found (a hit), it is read from the cache memory and no external bus cycle occurs. If the data is not found (a miss), an external bus cycle is used to read the data from system memory. If the address of the missed data is in cacheable address space, the data is stored in the cache memory and the remainder of the cache line is read.

When the microprocessor performs a memory write, the data address is used to search the cache. If the address is found (a hit), the data is written to the cache and no external bus cycle is used to write the data to system memory. (If the address of the write operation was not in the cache memory but was in cacheable address space, the data is read back into the cache memory and the remainder of the cache line is read.)

Cacheable Address Space

Cacheable address space is defined as system memory that resides on the system board (0–640 KB and 1 MB–256 MB). Cacheability of system memory is up to 64 MB for Pentium or 512 MB for Pentium II in the L2 cache. Nothing in address range hex A0000–BFFFF, I/O address space, or memory in any AT slot is cached.

ROM address space (hex C0000–C9FFF and F0000–FFFFFF) is L1 cacheable for *code read operations only*. If data in this address range is already in cache memory and the address range is written to, the cached line is invalidated and is read again from RAM, where the BIOS is shadowed.

Bus Adapter

When the computer is attached to the ThinkPad SelectaDock III docking system, the PCI adapters or AT-bus adapters can be used through the docking system.

Keyboard/Mouse Connector

Each ThinkPad computer has a keyboard/mouse connector, where the IBM mouse, keyboard, or numeric keypad is connected.

Signals

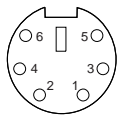
The keyboard and mouse signals are driven by open-collector drivers pulled to 5 V dc through a pull-up resistor. Figure 2-1 lists the signals.

Sink current	1 mA	Maximum
High-level output voltage	5.0 V dc minus pullup	Minimum
Low-level output voltage	0.5 V dc	Maximum
High-level input voltage	2.0 V dc	Minimum
Low-level input voltage	0.8 V dc	Maximum

Figure 2-1. Keyboard and Mouse Signals

Connector

The keyboard/mouse connector uses a 6-pin, miniature DIN connector.



Pin	I/O	Signal Name
1	I/O	Mouse Data
2	I/O	Keyboard Data
3	–	Ground
4	–	+5 V dc
5	I/O	Mouse Clock
6	I/O	Keyboard Clock

Figure 2-2. Keyboard/Mouse Connector Pin Assignments

Note: The maximum current for +5 V dc (pin 4) is 0.5 A.

Scan Codes

Figure 2-3 shows the key numbers assigned to keys on the 85-key keyboard (for the U.S.).

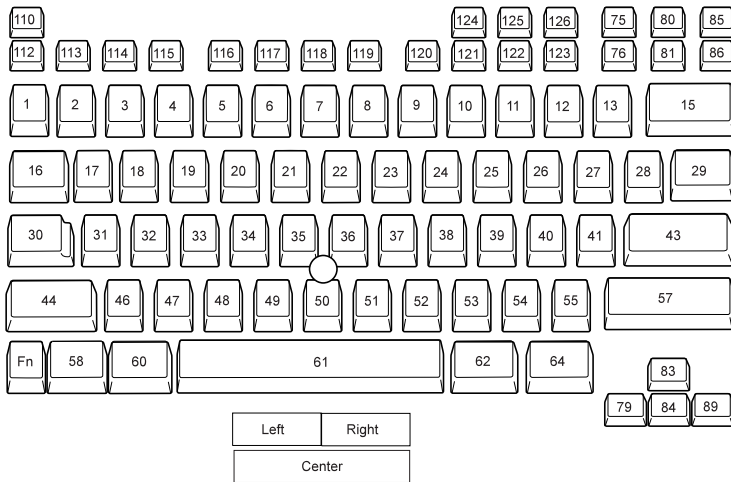


Figure 2-3. Key Numbers for the 85-Key Keyboard

Figure 2-4 shows the key numbers assigned to keys on the 86-key keyboard (for countries other than the U.S. and Japan).

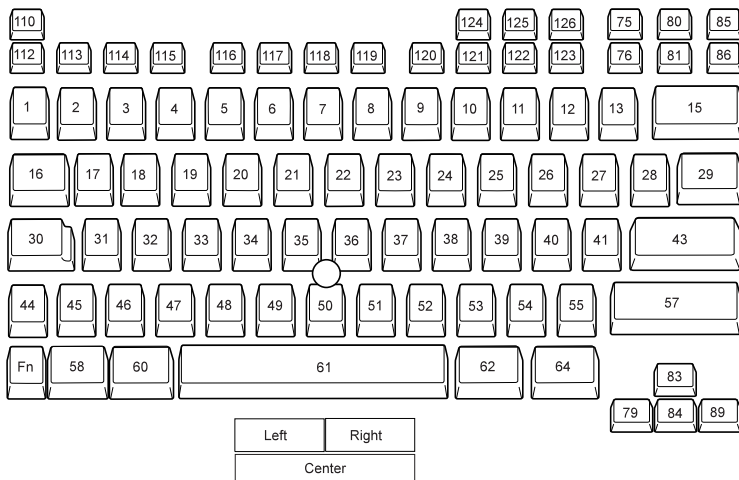


Figure 2-4. Key Numbers for the 86-Key Keyboard

Figure 2-5 on page 2-6 shows the key numbers assigned to the keys on the 90-key keyboard (for Japan).

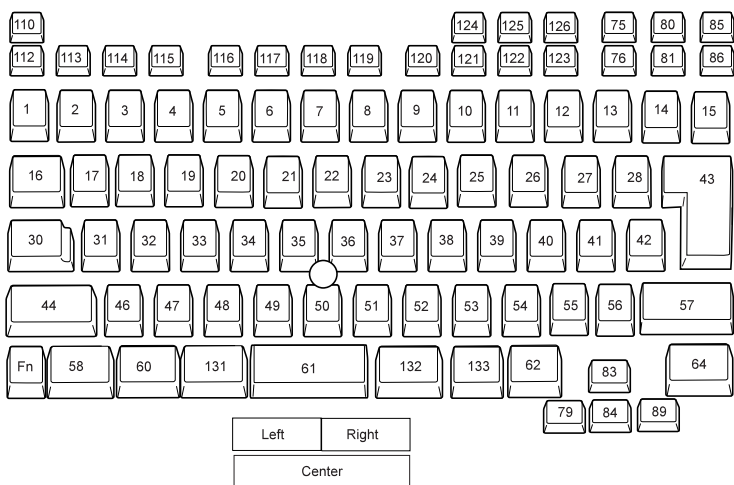


Figure 2-5. Key Numbers for the 90-Key Keyboard

For scan codes assigned to each numbered key, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Keyboard ID

The keyboard ID consists of 2 bytes: hex 83AB (the built-in keyboard with the external numeric keypad) or hex 84AB (the built-in keyboard only). Interrupt 16H, function code (AH)=0AH, returns the keyboard ID in BX.

Figure 2-6 shows the key numbers assigned to keys on the external numeric keypad. For scan codes assigned to each numbered key, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

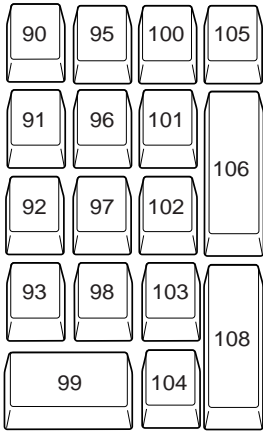


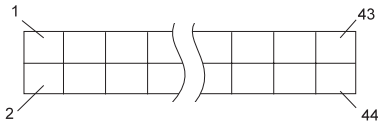
Figure 2-6. Key Numbers for the External Numeric Keypad

Displayable Characters and Symbols

For displayable characters and symbols that are keyable from the keyboard, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Hard Disk Drive Connector

The hard disk drive connected to the system board is removable. Figure 2-7 shows the pin assignments for the connector on the system board.



Pin	Signal	I/O or Feature	Pin	Signal	I/O or Feature
1	RSTDRVI	O	2	GND	Ground
3	PDD7	I/O	4	PDD8	I/O
5	PDD6	I/O	6	PDD9	I/O
7	PDD5	I/O	8	PDD10	I/O
9	PDD4	I/O	10	PDD11	I/O
11	PDD3	O	12	PDD12	I/O
13	PDD2	I/O	14	PDD13	I/O
15	PDD1	I/O	16	PDD14	I/O
17	PDD0	I/O	18	PDD15	I/O
19	GND	Ground	20	Key	NC
21	-PDREQ	I	22	GND	Ground
23	-PDIOW	O	24	GND	Ground
25	-PDIOR	O	26	GND	Ground
27	PIODRY	I	28	CSEL(GND)	0
29	-PDACK	O	30	GND	Ground
31	IRQ14	I	32	Reserved	NC
33	PDA1	O	34	-PDIAGHDD	I
35	PDAO	O	36	PDA2	O
37	-CS1P	Ground	38	-CS3P	O
39	-DASPHDD2	I	40	GND	Ground
41	VCC5B	Vcc	42	VCC5B	Vcc
43	GND	Ground	44	Reserved	NC

Figure 2-7. Hard Disk Drive Connector Pin Assignments

External Bus Connector

The docking station is connected through the 240-pin external bus connector on the rear panel. This connector is installed on the system board and has the following pin assignments:



Pin	Signal Name	Pin	Signal Name
001	VCC5A	061	Dock-PWR
002	VCC5A	062	Dock-PWR
003	-PCIRST_DOCK	063	Dock-PWR
004	-ACK_DOCK	064	Dock-PWR
005	-CLKRUN_DOCK	065	DOCK-L_OUT
006	GND	066	AGND
007	GND	067	DOCK-L_IN
008	AD30	068	XKBDATA
009	AD28	069	GND
010	AD26	070	GND
011	AD24	071	MSDATA
012	GND	072	MSCLK
013	GND	073	-TORI
014	AD23	074	-IOCTS
015	AD21	075	-IODTR
016	AD19	076	-IORXD
017	AD17	077	-PWRON
018	GND	078	AD0
019	GND	079	AD2
020	C_BE2	080	GND
021	-IRDY_DOCK	081	GND
022	-DEVSEL_DOCK	082	AD4
023	-LOCK_DOCK	083	AD6
024	GND	084	C_BE0
025	GND	085	GND
026	-SERR_DOCK	086	AD9
027	-PAR_DOCK	087	AD11
028	TDO	088	AD13
029	TMS	089	R_S
030	-TRST	090	-MOTENO
031	-BRRESET	091	TCLK
032	AD14	092	TDI
033	AD12	093	AD15
034	AD10	094	C_BE1
035	AD8	095	-PERR_DOCK
036	GND	096	-STOP_DOCK
037	GND	097	-TRDY_DOCK
038	AD7	098	GND
039	AD5	099	GND
040	AD3	100	-FRAME_DOCK
041	GND	101	GND
042	GND	102	AD16
043	AD1	103	AD18
044	PRDY	104	GND
045	-CPURST_DS	105	AD20
046	-IODCD	106	GND
047	IOTXD	107	AD22
048	-IORTS	108	C_BE3
049	-IODSR	109	GND
050	SAFE5V	110	GND
051	XKBCLK	111	AD25
052	GND	112	AD27
053	GND	113	AD29
054	DODK_R_IN	114	AD31
055	AGND	115	GND
056	DOCK_R_OUT	116	-REQ_DOCK
057	DOCK-PWR	117	PCICLK_DOCK
058	DOCK-PWR	118	-BATOPDSBL
059	DOCK-PWR	119	VCC5B
060	DOCK-PWR	120	VCC5B

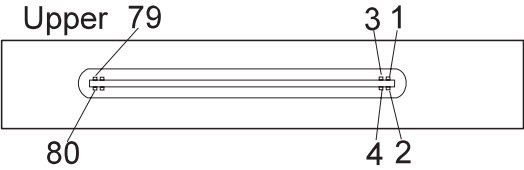
Figure 2-8 (Part 1 of 2). 240-Pin External Bus Connector Pin Assignments

Pin	Signal Name	Pin	Signal Name
121	GND	181	-DOCK_ID2
122	-DOCK_ID1	182	GND
123	IRQSER	183	USBP1-
124	IRQ5	184	UDBP1+
125	IRQ7	185	GND
126	IRQ10	186	GND
127	IRQ11	187	12C_DATA
128	IRQ14	188	JBCY
129	-INTB_DOCK	189	JBCX
130	-INTC_DOCK	190	JBB2
131	-INTD_DOCK	191	VTTON
132	-DASPDOCK	192	JBB1
133	GND	193	MIDIOUT_DOCK
134	GND	194	MIDIIN_DOCK
135	CRTID0	195	GND
136	CDTID2	196	GND
137	DDCCLK_ID3	197	-PWRSWITCH
138	GND	198	-BUSSUSSTAT
139	CRT_RED	199	-PCMCIAI4
140	LPTSLECT	200	-SIDE1SEL
141	LPTPE	201	DRATE0
142	LPTBUSY	202	-WREN
143	LPTD7	203	-DRVID1
144	LPTD6	204	-DIR
145	LPTD3	205	-MOTEN1
146	LPTD2	206	GND
147	LPTD1	207	-DISKCHG
148	LPTD0	208	-INDEX_1
149	-LPTAFD	209	-PDDATA_1
150	GND	210	GND
151	GND	211	GND
152	GND	212	-LPTSTB
153	-LPTERR	213	-LPTINIT
154	-WRDATA_1	214	-LPTSLIN
155	-DRVSEL1	215	LPTD4
156	-DRVID0	216	LPTD5
157	-MEDID0	217	GND
158	DRATE1	218	GND
159	-STEP	219	-LPTACK
160	GND	220	GND
161	-MEDID1	221	CRT_GREEN
162	-TRACK0	222	GND
163	-WPROTECT	223	CRT_BLUE
164	GND	224	DDCDATA_ID1
165	GND	225	CRT_VSYNC_EXT
166	LAST_PWG	226	CRT_HSYNC_EXT
167	-EVENT	227	GND
168	DOCK_SPKR	228	GND
169	JAB1	229	-PHLDA_DOCK
170	JAB2	230	-PHLD_DOCK
171	JACX	231	-INTA_DOCK
172	JACY	232	IDE2IRQ
173	12C_CLK	233	IRQ15
174	GND	234	IRQ12
175	GND	235	IRQ9
176	SUSCLK	236	IRQ6
177	-PCIPME	237	IRQ4
178	USB_OC1	238	IRQ3
179	GND	239	GND
180	-DOCK_ID3	240	-DOCK_ID0

Figure 2-8 (Part 2 of 2). 240-Pin External Bus Connector Pin Assignments

UltraSlim Bay Connector

The removable diskette drive or CD-ROM drive can be connected to the UltraSlim Bay connector on the system board. This connector has the following pin assignments.



Pin	Signal	I/O and Feature
1	-UBAYID1	I
2	-UBAYID2	I
3	GND	GND
4	GND	GND
5	-INDEX	I
6	-DRVSELO	O
7	-DISKCHG	I
8	-DRVID0	I
9	NC	N/C
10	-MEDID0	I
11	-MONTENO	O
12	DRATE1	O
13	-DIR	O
14	-DRVID1	I
15	-STEP	O
16	GND	GND
17	-WRDATA	O
18	GND	GND
19	-WREN	O
20	-MEDID1	I
21	-TRACK0	I
22	DRATE0	O
23	-WPROTECT	I
24	-RDDATA	I
25	GND	GND
26	-SIDE1SEL	O
27	-UBAYID0	O
28	BAYRESET	O
29	GND	GND
30	SDD7	I/O
31	SDD8	I/O
32	SDD6	I/O
33	SDD9	I/O
34	GND	GND
35	SDD5	I/O
36	DD10	I/O
37	SDD4	I/O
38	SDD11	I/O
39	VCC5B	VCC
40	VCC5B	VCC
41	VCC5B	VCC
42	VCC5B	VCC
43	SDD3	I/O
44	SDD12	I/O
45	SDD2	I/O
46	SDD13	I/O
47	GND	GND
48	SDD1	I/O
49	SDD14	I/O
50	SDD0	I/O

Figure 2-9 (Part 1 of 2). UltraSlim Bay Connector Pin Assignments

Pin	Signal	I/O and Feature
51	SDD15	I/O
52	GND	GND
53	UBAYID0	I
54	-SDREQ	I
55	GND	GND
56	-SDIOW	O
57	GND	GND
58	-SDIOR	O
59	GND	GND
60	SIORDY	I
61	UBAYSLAVE	O
62	-SDACK	O
63	IRQ	I
64	Reserved	I
65	SDA1	O
66	-PDIAGHDD	I/O
67	SDA0	O
68	SDA2	O
69	-CS1S	O
70	-CS3S	O
71	-DASPUBAY	I
72	-MCS	O
73	CD_MUTE	I
74	AUDIO_RTN	I
75	CD_L_IN	I
76	CD_R_IN	I
77	GND	GND
78	GND	GND
79	-UBAYID3	I
80	-UBAYID4	I

Figure 2-9 (Part 2 of 2). UltraSlim Bay Connector Pin Assignments

Diskette Drive and Controller

Figure 2-10 shows the read, write, and format capabilities of the diskette drive for the ThinkPad computer.

Diskette Type	Format Size		
	720 KB	1.2 MB	1.44 MB
3.5-inch 1.0 MB Diskette	RWF	–	–
3.5-inch 2.0 MB Diskette	–	RWF	RWF
Legend:			
1 KB (kilobyte)	1024 bytes		
1 MB (megabyte)	1,048,576 bytes		
R	Read		
W	Write		
F	Format		

Figure 2-10. Diskette Drive Read, Write, and Format Capabilities

Memory

The ThinkPad computers use the following types of memory:

- Read-only memory (ROM)

- Random access memory (RAM)

- Real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS RAM)

ROM Subsystem

The ROM subsystem consists of four banks of 128-KB memory. ROM is active when power is turned on and is assigned to the top of the first and last 1 MB of address space (hex 000F0000–000FFFFF and hex FFFF0000–FFFFFFFF). After POST checks that system memory is operating correctly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 00000000 of the address space. The RAM subsystem for the ThinkPad 600 computer is 64 bits wide.

The 32-MB base memory is on the system board. Two 144-pin 8-byte dual inline memory module (DIMM) connectors are provided on the system board. Both connectors accept an 8-MB, a 16-MB, a 32-MB, or a 64-MB DIMM. The memory capacity can be increased up to 160 MB.

The total amount of usable memory is less than the amount of memory installed because of ROM-to-RAM remapping and power management.

System Memory Map

Memory is mapped by the memory controller registers.

Figure 2-11 shows the memory map for a correctly functioning system. Memory can be mapped differently if POST detects an error in system board memory or RT/CMOS RAM. In the figure, the variable *x* represents the number of 1-MB blocks of system board memory starting at or above the hex 100000 boundary.

Hex Address Range	Function
00000000 to 0009FFFF	640-KB system board RAM
000A0000 to 000BFFFF	Video RAM
000C0000 to 000C9FFF	System board video BIOS ROM mapped to RAM
000C8000 to 000EFFFF	Channel ROM
000F0000 to 000FFFFF	64-KB system board ROM mapped to RAM
00100000 to (00100000 + <i>x</i> MB)	<i>x</i> MB system board RAM
FFFF0000 to FFFFFFFF	64-KB system board ROM (same as 000F0000 to 000FFFFF)

Figure 2-11. System Memory Map

System Board Memory for the DIMM Connectors

The system board has two DIMM connectors.

Figure 2-12 shows the pin assignments for the DIMM connector.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	38	DQ40	75	Vss	110	A12
2	Vss	39	DQ9	76	Vss		(BS1)
3	DQ0	40	DQ41	77	Reserved	111	A10
4	DQ32	41	DQ10	78	Reserved		(AP)
5	DQ1	42	DQ42	79	Reserved	112	A13
6	DQ33	43	DQ11	80	Reserved	113	Vcc
7	DQ2	44	DQ43	81	Vcc	114	Vcc
8	DQ34	45	Vcc	82	Vcc	115	DQMB2
9	DQ3	46	Vcc	83	DQ16	116	DQMB6
10	DQ35	47	DQ12	84	DQ48	117	DQMB3
11	Vcc	48	DQ44	85	DQ17	118	DQMB7
12	Vcc	49	DQ13	86	DQ49	119	Vss
13	DQ4	50	DQ45	87	DQ18	120	Vss
14	DQ36	51	DQ14	88	DQ50	121	DQ24
15	DQ5	52	DQ46	89	DQ19	122	DQ56
16	DQ37	53	DQ15	90	DQ51	123	DQ25
17	DQ6	54	DQ47	91	Vss	124	DQ57
18	DQ38	55	Vss	92	Vss	125	DQ26
19	DQ7	56	Vss	93	DQ20	126	DQ58
20	D39	57	Reserved	94	DQ52	127	DQ27
21	Vss	58	Reserved	95	DQ21	128	DQ59
22	Vss	59	Reserved	96	DQ53	129	Vcc
23	DQMB0	60	Reserved	97	DQ22	130	Vcc
24	DQMB4	61	CK0	98	DQ54	131	DQ28
25	DQMB1	62	CKEA	99	DQ23	132	DQ60
26	DQMB5	63	Vcc	100	DQ55	133	DQ29
27	Vcc	64	Vcc	101	Vcc	134	DQ61
28	Vcc	65	/RAS	102	Vcc	135	DQ30
29	A0	66	/CAS	103	A6	136	DQ62
30	A3	67	/WE	104	A7	137	DQ31
31	A1	68	CKEB	105	A8	138	DQ63
32	A4	69	/S0	106	A11	139	Vss
33	A2	70	CKEB		(BS0)	140	Vss
34	A5	71	/S1	107	Vss	141	SDA
35	Vss	72	RFU	108	Vss	142	SCL
36	Vss	73	RFU	109	A9	143	Vcc
37	DQ8	74	CK1			144	Vcc

Figure 2-12. DIMM Adapter Card Memory Connector Pin Assignments

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) module contains the real-time clock and 128 bytes of CMOS RAM. The clock circuitry uses 14 bytes of this memory; the remainder is allocated to configuration and system-status information. A battery is built into the module to keep the RT/CMOS RAM active when the power supply is not turned on. In addition to the 128 bytes of CMOS/RAM, a CMOS/RAM extension of 4 KB is provided for configuration and other system information.

Figure 2-13 lists the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-time clock
00E	Diagnostic status
00F	Shutdown status
010	Diskette drive type
011	Hard disk 2 and 3 drive type
012	Hard disk 0 and 1 drive type
013	Reserved
014	Equipment
015, 016	Low and high base memory
017, 018	Low and high expansion memory
019	Hard disk 0 extended byte
01A	Hard disk 1 extended byte
01B	Hard disk 2 extended byte
01C	Hard disk 3 extended byte
01D–02D	Reserved
02E, 02F	Checksum
030, 031	Low and high usable memory above 1 MB
032	Date-century
033–07F	Reserved

Figure 2-13. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

The NMI mask register is used with the RT/CMOS data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Attention

The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent failures of the RT/CMOS RAM can occur.

Bit	Function
7	NMI mask
6–0	RT/CMOS RAM address

Figure 2-14. RT/CMOS Address and NMI Mask Register (Hex 0070)

Bit 7 When this write-only bit is set to 1, the NMI is masked (disabled). This bit is set to 1 by a power-on reset.

Bits 6–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

The RT/CMOS data register is used with the RT/CMOS address and NMI mask register (hex 0070) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 2-15. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, you should mask interrupts to prevent other interrupt routines from changing the RT/CMOS address register before data is read or written. After I/O operations, you should leave the RT/CMOS address and NMI mask register (hex 0070) pointing to status register D (hex 00D).

Attention

The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent failures of the RT/CMOS RAM can occur.

Writing to the RT/CMOS RAM requires the following:

1. Write the RT/CMOS RAM address to the RT/CMOS address and NMI mask register (hex 0070).
2. Write the data to the RT/CMOS data register (hex 0071).
3. Write the address, hex 0F, to the RT/CMOS and NMI mask register; this leaves hex 0070 pointing to the shutdown status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS.

Reading from the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI mask register (hex 0070).
2. Read the data from the RT/CMOS data register (hex 0071).
3. Write the address, hex 0F, to the RT/CMOS and NMI mask register; this leaves hex 0070 pointing to the shutdown status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000–00D): Bit definitions and addresses for the real-time clock bytes are shown in Figure 2-16.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status register A	10
00B	Status register B	11
00C	Status register C	12
00D	Status register D	13

Figure 2-16. Real-Time Clock Bytes (Hex 000–00D)

Note: The setup program initializes status registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface to read and set the time and date; it initializes the registers in the same way that the setup program does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress (UIP)
6-4	Division Chain Select (DVx)
3-0	Rate-selection bits

Figure 2-17. Status Register A (Hex 00A)

Bit 7 This bit is a status flag that can be monitored. If this bit is 1, the update transfer will soon occur. If this bit 0, the update transfer will not occur for at least 244 μ s.

Bits 6–4 These bits control the divider chain for the oscillator.

Bits 3–0 These bits allow the selection of a divider output frequency or disable the divider output.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic interrupt
5	Enable alarm interrupt
4	Enable update-ended interrupt
3	Enable square wave
2	Date mode
1	24-hour mode
0	Enable daylight-saving time

Figure 2-18. Status Register B (Hex 00B)

- Bit 7** If set to 0, this bit updates the cycle, normally by advancing the count at a rate of one cycle per second. If set to 1, it immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.
- Bit 6** This is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in status register A. If set to 1, this bit enables the interrupt. The system initializes this bit to 0.
- Bit 5** If set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.
- Bit 4** If set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.
- Bit 3** If set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in status register A. The system initializes this bit to 0.
- Bit 2** This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. If set to 1, this bit indicates binary format. The system initializes this bit to 0.
- Bit 1** This bit indicates whether the hours byte is in 12-hour or 24-hour mode. If set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.
- Bit 0** If set to 1, this bit enables the daylight-saving-time mode. If set to 0, this bit disables the daylight-saving-time mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt request flag
6	Periodic interrupt flag
5	Alarm interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 2-19. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in status register B.

Bit 7 If set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 If set to 1, this bit indicates that a periodic interrupt has occurred.

Bit 5 If set to 1, this bit indicates that an alarm interrupt has occurred.

Bit 4 If set to 1, this bit indicates that an update-ended interrupt has occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 2-20. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the internal battery. If set to 1, this bit indicates that the real-time clock has power. If set to 0, it indicates that the real-time clock has lost power and the data in CMOS is no longer valid.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

Figure 2-21 shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory size mismatch
3	Hard disk controller/drive C initialization status
2	Time status indicator
1, 0	Reserved

Figure 2-21. Diagnostic Status Byte (Hex 00E)

- Bit 7** If set to 1, this bit indicates that the real-time clock has lost power.
- Bit 6** If set to 1, this bit indicates that the checksum is incorrect.
- Bit 5** This bit indicates the results of a power-on check of the equipment byte (hex 014). If set to 1, this bit indicates that the configuration information is incorrect.
- Bit 4** If set to 1, this bit indicates that the memory size does not match the configuration information.
- Bit 3** If set to 1, this bit indicates that the controller or hard disk drive failed initialization.
- Bit 2** If set to 1, this bit indicates that the time is invalid.
- Bits 1, 0** These bits are reserved.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of the installed diskette drive.

Bit	Drive Type
7-4	Diskette drive type
3-0	Reserved

Figure 2-22. Diskette Drive Type Byte (Hex 010)

Bits 7-4 These bits indicate the diskette drive type.

Bits 7-4	Description
0 1 1 0	Diskette drive (2.88MB)
0 1 0 0	Diskette drive (1.44MB)
Note: Combinations not shown are reserved.	

Figure 2-23. Diskette Drive Type Bits 7-4

Bits 3-0 These bits are reserved.

Hard Disk Drive Type Byte (Hex 011): This byte defines the type of hard disk drive installed. Hex 00 indicates that no hard disk drive is installed.

Bit	Drive Type
7-4	Hard disk drive type 2
3-0	Hard disk drive type 3

Figure 2-24. Hard Disk Type Byte (Hex 011)

Bit 7-4	Description
0 0 0 0	No drive installed for hard disk drive 2
1 1 1 1	Use CMOS 1BH for hard disk drive 2

Figure 2-25. Hard Disk Drive Type 2 (Bits 7-4)

Bit 3-0	Description
0 0 0 0	No drive installed for hard disk drive 3
1 1 1 1	Use CMOS 1CH for hard disk drive 3

Figure 2-26. Hard Disk Drive Type 3 (Bits 3-0)

Hard Disk Drive Type Byte (Hex 012): This byte defines the type of hard disk drive installed. Hex 00 indicates that no hard disk drive is installed.

Bit	Drive Type
7-4	Hard disk drive 0
3-0	Hard disk drive 1

Figure 2-27. Hard Disk Drive Type Byte

Reserved Bytes (Hex 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Description
7, 6	Number of diskette drives
5, 4	Display operating mode
3, 2	Reserved
1	Coprocessor presence
0	Diskette drive 0 presence

Figure 2-28. Equipment Byte

Bits 7, 6 These bits indicate the number of installed diskette drives.

Bits 7,6	Number of Diskette Drives
0 0	One drive
0 1	Reserved
1 0	Reserved
1 1	Reserved

Figure 2-29. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port.

Bits 5,4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 2-30. Display Operating Mode Bits

Bits 3–2 These bits are reserved.

Bit 1 If set to 1, this bit indicates that a coprocessor is installed.

Bit 0 If set to 1, this bit indicates that physical diskette drive 0 is installed.

Low and High Base Memory Bytes (Hex 015 and Hex 016): The low and high base memory bytes define the amount of memory below the 640-KB address space.

The value in these bytes represents the number of 1-KB blocks of base memory. For example, hex 0280 indicates 640 KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion Memory Bytes (Hex 017 and Hex 018): The low and high expansion memory bytes define the amount of memory above the 1-MB address space.

The value in these bytes represents the number of 1-KB blocks of expansion memory. For example, hex 0800 indicates 2048 KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 01D–02D): These bytes are reserved.

Configuration Checksum Bytes (Hex 02E and Hex 02F): The configuration checksum bytes contain the checksum character for bytes hex 010 through hex 02D of the 64-byte CMOS RAM. The high byte is hex 02E; the low byte is hex 02F.

Low and High Usable Memory Bytes (Hex 030 and Hex 031): The low and high usable memory bytes define the total amount of contiguous memory from 1 MB to 20 MB.

The hexadecimal values in these bytes represent the number of 1-KB blocks of usable memory. For example, hex 0800 is equal to 2048 KB. The low byte is hex 30; the high byte is hex 31.

Date-Century Byte (Hex 032): Bits 7 through 0 of the date-century byte contain the binary-coded decimal value for the century. For information about reading and setting this byte, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface*.

Reserved Bytes (Hex 033–07F): These bytes are reserved.

Miscellaneous System Functions and Ports

This section provides information about nonmaskable interrupts (NMIs), the power-on password, and hardware compatibility.

Nonmaskable Interrupt (NMI)

The NMI signals the system microprocessor that a channel check timeout has occurred. This situation can cause lost data or an overrun error on some I/O devices. The NMI masks all other interrupts. The interrupt return (IRET) instruction restores the interrupt flag to the state it was in before the interrupt occurred. A system reset causes a reset of the NMI.

The NMI requests from a system board channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. See “RT/CMOS Address and NMI Mask Register (Hex 0070)” on page 2-19. The power-on default of the NMI mask is 1 (NMI disabled).

Attention

The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent failures of the RT/CMOS RAM can occur.

System Control Port A (Hex 0092)

Bit	Function
7-4	Reserved
3	Security lock latch
2	Reserved (must be set to 0)
1	Alternate gate A20
0	Alternate hot reset

Figure 2-31. System Control Port A (Hex 0092)

Bits 7-4 These bits are reserved.

Bit 3 This bit provides a security lock for the secured area of RT/CMOS. If this bit is set to 1, the 8-byte power-on password is locked by the software. After this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. If this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems requiring faster operation than that provided on the IBM Personal Computer AT. Resetting the system microprocessor switches the microprocessor from protected mode to real address mode.

This bit is set to 0 by either a system reset or a write operation. If a write operation changes this bit from 0 to 1, the 'processor reset' signal is pulsed after the reset has occurred. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is set to 0, POST assumes that the system was just powered on. If the bit is set to 1, POST assumes that the microprocessor has been switched from protected mode to real mode.

If bit 0 is used to reset the system microprocessor to the real mode, use the following procedure:

1. Disable all maskable and nonmaskable interrupts.

2. Reset the system microprocessor by writing a 1 to bit 0.
3. Issue a Halt instruction to the system microprocessor.
4. Reenable all maskable and nonmaskable interrupts.

If you do not follow this procedure, the results are unpredictable.

Note: Whenever possible, use BIOS as an interface to reset the system microprocessor to the real mode. For more information about resetting the system microprocessor, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface*.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures:

Bit	Function
7-4	Reserved
3	Enable channel check
2	Enable PCI SERR#
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 2-32. System Control Port B (Hex 0061, Write)

Bit	Function
7	PCI SERR# (PCI error) status
6	Channel check status
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable PCI SERR# (PCI error) check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 2-33. System Control Port B (Hex 0061, Read)

Bit 7 If a system board error occurs and the PCI SERR# line is activated, this bit is set to 1.

- Bit 6** If set to 1, this bit indicates that a channel check has occurred.
- Bit 5** If read, this bit indicates the condition of the timer/counter 2 'output' signal.
- Bit 4** If read, this bit toggles for each refresh request.
- Bit 3** If set to 0, this bit enables the channel check. This bit is set to 1 during a power-on reset.
- Bit 2** If set to 0, this bit enables the PCI SERR#.
- Bit 1** If set to 1, this bit enables the speaker data.
- Bit 0** If set to 1, this bit enables the timer 2 gate.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and the check character. The 8 bytes are initialized to hex 00. The microprocessor can access these bytes only during POST. After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by any program.

During power-on password installation, the password (1 to 7 characters) is stored in the security space.

Installing the password is a function of the built-in system program *Easy-Setup*. The power-on password does not appear on the screen when it is installed, changed, or removed. After the power-on password has been installed, it can be changed or removed only during POST.

The computer also can have a keyboard password. For more information, see the keyboard and auxiliary device controller section of the *IBM Personal System/2 Hardware Interface Technical Reference*.

Other Passwords

In addition to the power-on password, the computer provides two more passwords:

The **hard-disk password** (HDP) protects the data on your removable hard disk drive from being accessed by unauthorized persons.

The **supervisor password** protects the system information in Easy-Setup from being changed by unauthorized persons.

For more information about these passwords, refer to the *ThinkPad User's Guide*.

Selectable Drive-Startup Sequence

Selectable drive-startup (selectable boot) allows you to control the startup sequence of the drives in your computer. The order in which the computer looks for the drives for your operating system is the *drive-startup sequence*. If you are working with multiple operating systems, you might want to change the drive-startup sequence to load the operating system from the hard disk without first checking the diskette drive, or to do a remote program load (RPL).

Attention

When changing your startup sequence, you must be extremely careful when doing write operations (such as copying, saving, or formatting). Your data or programs can be overwritten if you select the wrong drive.

For more information about the selectable drive-startup sequence, refer to the *ThinkPad User's Guide*.

Hardware Compatibility

The computer supports most of the interfaces used by the IBM Personal Computer AT* and the Personal System/2* (PS/2*) products. In many cases, the command and status organization of these interfaces is maintained.

The functional interfaces for the computer are compatible with the following:

- The Intel 8259 interrupt controllers (edge trigger mode).

- The Intel 8254 timers driven from 1.193 MHz (channels 0, 1, and 2).

- The Intel 8237 DMA controller-address/transfer counters, page registers, and status fields only. The command and request registers, and the rotate and mask functions, are not supported. The mode register is partially supported.

- The NS16550 serial communications controller.

- The Intel Pentium microprocessor.

- The Intel 8086**, 8088**, 80286**, 80386**, and i486DX microprocessors.

- The Intel 8087**, 80287**, and 80387** math coprocessors.

- The Intel 82077AA** diskette drive controller.

- The keyboard interface at addresses hex 0060 and hex 0064.

- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.

Error Codes

POST returns a three or more character code message to indicate which test failed. Figure 2-34 lists the failure indicated with the associated error code.

Error Code	Description
101	Interrupt failure.
102	Timer failure.
103	Timer interrupt failure.
104	Protected mode failure.
105	Last 8042 command not accepted.
107	NMI test failure.
108	Timer bus test failure.
109	Low meg-chip select test.
110	Planar parity.
111	I/O parity.
118	Planar parity error logged.
127	Cache error.
158	A supervisor password is set, but no hard disk password is set.
159	The hard disk password is not identical to the supervisor password.
161	Dead battery.
162	Check sum or configuration error.
163	Date and time are not set; clock not updated.
173	CMOS CRC error.
174	Configuration error.
175	Bad EEPROM CRC 1.
177	Bad supervisor password checksum.
178	EEPROM is not functional.
179	NVRAM error log full.
183	Supervisor password is needed.
184	Bad power-on password checksum.
185	Corrupted startup boot sequence.
186	Inconsistency between EEPROM and security lock latch 2.
188	Bad EEPROM CRC 2.
190	Critically low battery condition detected.
191	PM general error.
192	Fan error.
195	Configuration mismatch error found during hibernation wake-up.
196	Critical error found during hibernation wake-up.
201	Memory data error.
202	Memory line error 00 through 15.
203	Memory line error 16 through 23.
215	Memory test failure on on-board memory.
221	ROM to RAM remap error.
225	Unsupported memory module is installed.
301	Keyboard error.

Figure 2-34 (Part 1 of 2). Error Codes

Error Code	Description
601	Diskette drive or controller error.
602	No valid boot record on diskette.
604	Invalid diskette drive error.
1101	Serial-A test failure.
1201	Serial-B test failure.
1701	Hard disk controller failure.
1780, 1790	Hard disk 0 error.
1781, 1791	Hard disk 1 error.
2401	System board video error.
8081	PCMCIA presence test failure (PCMCIA revision number also checked).
8082	PCMCIA register test failure.
8601	System bus error (8042 mouse interface).
8602	External mouse error.
8603	System bus error or mouse error.
8611	System bus error (I/F between 8042 and IPDC).
8612	TrackPoint error.
8613	System board or TrackPoint error.
I9990301	Hard disk error.
I9990302	Invalid hard disk boot record.
I9990303	Bank-2 flash ROM checksum error.
I9990305	No bootable device.

Figure 2-34 (Part 2 of 2). Error Codes

Section 3. Subsystems

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This section describes the video, DSP, audio, IR, and PCMCIA subsystems of the ThinkPad 600 computer.

Video Subsystem

The video subsystem consists of the XGA video controller, which interprets the monitor buffer. The video subsystem supports an IBM thin-film transistor (TFT) or High Performance Addressing (HPA) as follows:

LCD Type	VRAM Size	Color Depth		Resolution	
		On the LCD	On the External Monitor	On the LCD	On the External Monitor
XGA TFT XGA HPA	2 MB	65,536	16,777,216	1024×768	640×480 800×600 1024×768

The video subsystem also supports PS/2 analog displays without any additional adapters.

Color	Resolution
65,536 colors	640×480
	800×600
	1024×768
16,777,216 colors	640×480
	800×600

Video Modes

The video subsystem supports the modes listed in Figure 3-1 and Figure 3-2 on page 3-4:

Mode (Hex)	Type	Colors	Alpha-numeric Format	Buffer Start Address	Box Size	Max Pages	Pels
0, 1	A/N	16	40x25	B8000	8x8	8	320x200
0*, 1*	A/N	16	40x25	B8000	8x14	8	320x350
0#, 1#	A/N	16	40x25	B8000	8x16	8	320x400
2, 3	A/N	16	80x25	B8000	8x8	8	640x200
2*, 3*	A/N	16	80x25	B8000	8x14	8	640x350
2#, 3#	A/N	16	80x25	B8000	8x16	8	640x400
4, 5	APA	4	40x25	B8000	8x8	1	320x200
6	APA	2	80x25	B8000	8x8	1	640x200
7*	A/N	-	80x25	B0000	8x14	8	640x350
7#	A/N	-	80x25	B0000	8x16	8	640x400
D	APA	16	40x25	A0000	8x8	8	320x200
E	APA	16	80x25	A0000	8x8	4	640x200
F	APA	-	80x25	A0000	8x14	2	640x350
10	APA	16	80x25	A0000	8x14	2	640x350
11	APA	2	80x30	A0000	8x16	1	640x480
12	APA	16	80x30	A0000	8x16	1	640x480
13	APA	256	40x25	A0000	8x8	1	320x200

Figure 3-1. BIOS Video VGA Modes

The following shows the video BIOS extended modes for the ThinkPad 600 computer (containing a NeoMagic NM2160 video chip, which interprets 2 MB VRAM):

Video Mode	VESA Mode Number (Hex)	External Monitor					LCD	
		60	70	75	85	XGA		
320x200x32k	10D						o	
320x200x64k	10E		o				o	
320x240x256	120		o				o	
320x240x64k	121						o	
400x300x256	122		o				o	
400x300x64k	123		o				o	
512x384x256	124		o				o	
512x384x64k	125						o	
640x400x256	100		o				o	
640x480x256	101						o	
640x480x32k	110		o				o	
640x480x64k	111		o				o	
640x480xTrue	112		o				o	
800x600x16	102		o				o	
800x600x256	103		o				o	
800x600x32k	113						o	
800x600x64k	114						o	
800x600xTrue	115						o	
1024x768x16	104		o				o	
1024x768x256	105		o				o	
1024x768x32k	116		o				o	
1024x768x64k	117		o				o	

Figure 3-2. Video BIOS Extended Modes—NeoMagic NM2160

Modem Subsystem

The modem subsystem is composed of a digital signal processor (DSP) and a data access arrangement (DAA):

- General MIDI-compatible, 40-voice wave table synthesizer
- 33.6-kbps data/fax modem
- Full-feature telephone
- Answering machine
- Headphone-free, full-duplex speaker phone

ThinkPad Modem

The modem subsystem provides three system settings: I/O address, IRQ level, and DMA channel.

I/O Address	IRQ Level	DMA Channel
0130–013F (default)	IRQ 3	DMA 0
0350–035F	IRQ 4	DMA 1
0770–077F	IRQ 5	DMA 6
0DB0–0DBF	IRQ 7	DMA 7 (default)
	IRQ 10 (default)	
	IRQ 11	
	IRQ 15	

MIDI Port Function

The MIDI port function provides one system setting:

I/O Address
0300–0303
0310–0313
0320–0323
0330–0333 (default)

Sound Blaster Support Function

The Sound Blaster support function provides three system settings: I/O address, IRQ level, and DMA channel.

I/O Address	IRQ Level	DMA Channel
0220–0233 (default)	IRQ 5 (default)	DMA 0
0240–0253	IRQ 7	DMA 1 (default)
0260–0273	IRQ 10	DMA 6
0280–0293	IRQ 11	DMA 7
0388–038B (synthesizer)		

Telephony (Modem) Function

The telephony (modem) function provides the following settings:

Serial Port
COM1 (I/O: 03F8 - IRQ 4)
COM2 (I/O: 02F8 - IRQ 3) (default)
COM3 (I/O: 03E8 - IRQ 4)
COM4 (I/O: 02E8 - IRQ 3)

Audio Subsystem

The crystal audio subsystem provides 16-bit stereo audio with high-quality FM music synthesis using four operators per voice. It can record, compress, and play back voice, sound, and music with built-in mixer controls. It consists of an embedded microprocessor, 16-bit stereo, 20-voice FM music synthesizer (or 18 simultaneous 4-operator voices), MIDI serial port compatible MPU401 UART mode, DMA control, and ISA bus interface logic.

The AudioDrive provides the computer with the following audio features:

- High-quality audio (44.1-kHz MPC-2 16-bit audio)
- General MIDI compatible, 32-voice wave table synthesizer
- Sound Blaster support

MIDI Port Function

The MIDI port I/O address is as follows (only when docked to the docking station):

I/O Address
0300–0301
0330–0331 (default)

Sound Blaster Support Function

The Sound Blaster support function provides three system settings: I/O address, IRQ level, and DMA channel.

I/O Address	IRQ Level	DMA Channel
0220–022F (default)	IRQ 5 (default)	DMA 0
0240–024F	IRQ 7	DMA 1 (default)
0338–038B (FM synthesizer)	IRQ 10	
	IRQ 11	

Audio Port Specifications

Audio Output:

- 1/8-inch mini-jack for headphone
- Headphone speaker output: 25 mW (32 Ω) maximum
- Maximum output level: 2.4 V pp
- Output impedance: 75 Ω

Audio Input:

- 1/8-inch mini-jack for microphone or line input
- Microphone gain: 34.3-dB maximum
- Maximum input level:
 - Microphone:** 570 mV rms
 - Line In:** 2 V rms
- Input impedance:
 - Microphone:** 8 k Ω
 - Line In:** 8 k Ω

Infrared (IR) Subsystem

The IR subsystem supports the following functions:

MIF/FIR mode

- 9.6 Kbps
- 57.6 Kbps
- 115.2 Kbps
- 1.152 Mbps
- 4.0 Mbps

Sharp** mode

- 9,600 bps

The I/O address can be selected from the following with the system utility program. The IR subsystem uses one serial port address and one IR controller register address:

I/O Address	
03F8–03FF	Serial port 1 (default)
02F8–02FF	Serial port 2
03E8–03EF	Serial port 3
02E8–02EF	Serial port 4
03F8–03FF	IR controller register 1 (default)
02F8–02FF	IR controller register 2
03E8–03EF	IR controller register 3
02E8–02EF	IR controller register 4

IRQ Level and DMA Channel

The IR subsystem uses one IRQ level and two DMA channels for ThinkPad mode. (Generic mode and Sharp mode do not require DMA channels.)

IRQ Level	DMA Channel
IRQ 3	DMA 0
IRQ 4 (default)	DMA 3
IRQ 5	

PC Card Subsystem

The system board has two PC Card slots that support the following types of PC Card:

- 16 bit PC Card Type-I, II, III 5V, 3.3V
- 32 bit PC Card Type-I, II, III 5V, 3.3V

DMA is not supported.

The maximum current per slot is:

- 500 mA at 5 V dc
- 500 mA at 3.3 V dc
- 50 mA at 12 V dc

The PCI1250 PCI-to-Cardbus Controller Unit¹ is used as the PC Card controller in the system unit. The available interrupt levels are IRQ 3, 4, 5, 7, 9, 10, 11, and 15.

The system unit resumes operation from suspend mode when it receives the 'RI_OUT' signal. The Type I and Type II PC Cards can be installed into either the upper or the lower slot, or into both slots at the same time. The Type III PC Card, however, must be installed only in the lower slot. The Type II PC card cannot be used in the upper slot when a Type III PC Card is used.

The PC Card slots are designed according to the PC Card standard released in March 1997.

¹ Manufactured by Texas Instruments Corporation.

Pin Assignments

Figure 3-3 shows the pin assignments for the PCMCIA slots.

Pin	16-Bit PC Card	32-Bit PC Card
1	Ground	Ground
2	D3	CAD0
3	D4	CAD1
4	D5	CAD3
5	D6	CAD5
6	D7	CAD7
7	CE1#	CC/BE0#
8	A10	CAD9
9	OE	CAD11
10	A11	CAD12
11	A9	CAD14
12	A8	CC/BE1#
13	A13	CPAR
14	A14	CPERR#
15	WE#	CGNT#
16	IRQ#	CINT#
17	Vcc	Vcc
18	Vpp	Vpp
19	A16	CCLK
20	A15	CIRDY#
21	A12	CC/BE2#
22	A7	CAD18
23	A6	CAD20
24	A5	CAD21
25	A4	CAD22
26	A3	CAD23
27	A2	CAD24
28	A1	CAD25
29	A0	CAD26
30	D0	CAD27

Figure 3-3 (Part 1 of 2). PCMCIA PC Card Slot Pin Assignments

Pin	16-Bit PC Card	32-Bit PC Card
31	D1	CAD29
32	D2	Reserved
33	IOIS16#	CCLKRUN#
34	Ground	Ground
35	Ground	Ground
36	CD1#	CCD1#
37	D11	CAD2
38	D12	CAD4
39	D13	CAD6
40	D14	Reserved
41	D15	CAD8
42	CE2	CAD10
43	VS1#	CVS1
44	IORD#	CAD13
45	IOWR#	CAD15
46	A17	CAD16
47	A18	Reserved
48	A19	CBLOCK#
49	A20	CSTOP#
50	A21	CDEVSEL#
51	Vcc	Vcc
52	Vpp	Vpp
53	A22	CTRDY#
54	A23	CFRAME#
55	A24	CAD17
56	A25	CAD19
57	AS2#	CVS2
58	RESET	CRST#
59	WAIT#	CSERR#
60	INPACK#	CREQ#
61	REG#	CC/BE3#
62	SPKR#	CAUDIO
63	STSCHG#	CSTSCHG
64	D8	CAD28
65	D9	CAD30
66	D10	CAD31
67	CD2#	CCD2#
68	GND	GND

Figure 3-3 (Part 2 of 2). PCMCIA PC Card Slot Pin Assignments

The maximum current for +5 V dc is .5 A for each slot (including both slots and V pp).

The maximum current for +12 V dc is .5 A for each slot (including both slots and V pp). When the computer is in suspend mode, it requires a current of 0.05 A.

IDE Channel on the UltraSlim Bay

A primary IDE channel is provided on the UltraSlim Bay connector, providing two system settings:

I/O Address	IRQ Level
01F0–01F7 03F6	IRQ 14

A secondary IDE channel is provided on the UltraSlim Bay connector, providing two system settings:

I/O Address	IRQ Level
0170–0177 0376	IRQ 15

If a hard disk is attached to the hard disk connector, an IDE device on the UltraSlim Bay becomes a primary slave. (The hard disk attached to the hard disk connector is the primary master.) If no hard disk is attached to the hard disk connector, an IDE device on the UltraSlim Bay is a primary master.

MIDI/Joystick Port

Note: To use a the MIDI/joystick port, you need a SelectaBase 600.

The MIDI/joystick port consists of the following functions:

- MIDI port (in/out)
- Joystick port

A standard game port connector is provided with a MIDI/joystick cable.

MIDI Interface

A MIDI communication function is provided with the DSP subsystem. The MIDI interface is compatible with MPU-401 (UART mode).

Joystick Interface

A joystick interface is provided at I/O address 0201. You can select whether to enable or disable it with the ThinkPad Configurations program.

Appendix A. System Resources

The following summarizes the available system resources for the computer and docking stations. Values in parentheses are alternative values that are selectable in the ThinkPad Configuration program or application programs. The default values are highlighted.

System Resource	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
Timer	0	0040–0043	None	None
Keyboard	1	0060 and 0064	None	None
Serial port	Disabled	Disabled	None	None
	4	03F8–03FF		
	3	02F8–02FF		
	4	03E8–03EF		
	3	02E8–02EF		
Parallel port	7	03BC–03BE (and 07BC–07BE)	None	0, 1, 3, or disabled
	7	0378–037F (and 0778–077A)		
	5	0278–027F (and 0678–067A)		
	Disabled	Disabled		
Infrared port	4, 3, or disabled	03F8–03FF , 02F8–02FF, 02E8–02EF, or 03E8–03EF	None	0 and 3 or disabled
Diskette controller	6	03F0–03F7	None	2
Video controller	None	03BA, 03B4–03B5, 03C0–03CF, 03D4–03D5, 03D8–03D9, 03DA, 2100–21FF, 2200–2203, 2300–2323	A0000–BFFFF and C0000–C9FFF	None
Sound Blaster	None	0220–022F , 0240–024F, 0260–0273, or 0280–0293	None	None

System Resource	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
MIDI	5, 7, 9, 10, 11, 15, or disabled	0330–0332, 0300–0302, 0310–0313, or 0320–0323	None	None
MIDI port	5, 7, 10, 11, or disabled	0330–0332 or 0300–0302	None	None
Joystick port	None	0201	None	None
(For models with internal modems only) ThinkPad modem	3	02F8–02FF	None	None
	4	03F8–03FF		
	4	03E8–03EF		
	3	02E8–02EF		
	Disabled	Disabled		
WSS codec base	5, 7, 9, 10, 11, 15	0530–0537, 0604–060B, 0E80–0E87, 0F40–0F47	None	0, 1, 3,
Video control base	None	0538–053F, 0D38–0D3F, 0E88–0E8F, 0FF0–0FF7	None	None
Hard disk drive, CD-ROM drive (for the CD-ROM drive model)	14 or 15	01F0–01F7 and 03F6, or 0170–0177 and 0376	None	None
PCMCIA controller	11	03E0–03E1 (the PC Card slot in the docking station: 03E2–03E3)	None	None
PC Card	(Dependent on the PC Card type)	(Dependent on the PC Card type)	(Dependent on the PC Card type)	None
Real time clock	8	0070–0071	None	None
TrackPoint or mouse	12	0060 and 0064	None	None
Math coprocessor exception	13	None	None	None

System Resource	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
SCSI controller SelectaDock I, SelectaDock II, SelectaDock III	11, 3, 4, 5, 7, 9, 10, 15, or disabled	Automatically set by the system	None	None
The IDE hard disk drive or IDE CD-ROM drive in the docking station	15, 10, 11	0170–0177 and 0376, 01F0–01F7 and 3F6, 01E8–01EF and 03EE, or 0168–016F and 036E	None	None
The ISA adapter card (option card) in the docking station	(Refer to the manual that came with the adapter card.)			
The PCI adapter card (option card) in the SelectaDock	11, 3, 4, 5, 7, 9, 10, 15, or disabled	(Refer to the adapter card manual.)		
<p>Note:</p> <p>The I/O addresses in parentheses are also used when ECP is enabled as the printer operating mode from the ThinkPad Configuration program.</p> <p>When you enable ECP as the printer operating mode from the ThinkPad Configuration program, you must select one value from the four selections (including “disabled”).</p> <p>Sound Blaster and MIDI share the same IRQ.</p> <p>IRQ 15 and I/O 0170–0177 and 0376 are applicable to the UltraSlim Bay devices only.</p>				

Appendix B. System Management API (SMAPI) BIOS Overview

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Overview

The ThinkPad Basic Input/Output System (BIOS) provides a special software interface, called the System Management Application Program Interface (SMAPI) BIOS, to control the following unique features of the ThinkPad system:

System Information

This BIOS provides unique ThinkPad information, such as the system identifier (system ID).

System Configuration

The ThinkPad SMAPI BIOS provides system configuration control for such features as display device selection or resource configuration for built-in devices.

Power Management

Through the SMAPI BIOS, the operating system or application software can control the ThinkPad power management features (the power mode or suspend/hibernation/resume options).

“Header Image” on page B-4 describes how to use the SMAPI BIOS.

Header Image

Systems that support SMAPI BIOS must provide the following header image in the F000 segment system ROM area at the 16-byte boundary. The client needs to search and find this SMAPI BIOS header image to get the entry point for the service.

Field	Offset (in Hex)	Length	Value
Signature	00	4 bytes	'\$SMB' (ASCII)
Version (Major)	04	Byte	01h
Version (Minor)	05	Byte	00h
Length	06	Byte	20h
Checksum	07	Byte	–
Information Word	08	Word	–
Reserved 1	0A	Word	–
Real mode 16-bit offset to entry point	0C	Word	–
Real mode 16-bit code segment address	0E	Word	–
Reserved 2	10	Word	–
16-bit protected mode offset to entry point	12	Word	–
16-bit protected mode code segment base address	14	Double words	–
32-bit protected mode offset to entry point	18	Double words	–
32-bit protected mode code segment base address	1C	Double words	–

Signature ASCII Code '\$SMB' is stored at the top of the header image.

Version (Major or Minor) Indicates the SMAPI BIOS version.

Length The length of the header image.

Checksum Checksum byte area. The client verifies that this header image is valid by using this checksum; the client should check all header image bytes, and the result will be zero bytes.

Information Word

This area identifies the following BIOS service level:

Information Word

Bit : Real/V86 mode interface support
Bit 1 : 16-bit protected mode support
Bit 2 : 32-bit protected mode support
Bit 3-15 : Reserved

Real Mode Entry Point

The entry point is specified in segment, offset format. Clients using Real/V86 mode can use this area for the far-call value.

16-Bit or 32-Bit Protected Mode Entry Point

The code base code address specifies the physical address for this BIOS, and the client must prepare the selector for this BIOS. The length should be 64 KB.

Calling Convention

The client can invoke the SMAPI BIOS with a far-call to the entry point that is specified in the header file. All parameters for the BIOS and other results are stored in the client data area; the client needs to prepare an input parameter and output parameter area in its data area, and informs this area by pushing those pointers onto its stack before the far-calls.

The SMAPI BIOS uses the stack/data area directly with the selector when the BIOS is invoked. Therefore, the caller needs to define the same privilege level as the BIOS.

Parameter Structure

The memory allocation for the input/output field should be prepared by the caller. The input field specifies the function request to the SMAPI BIOS, and the BIOS fills in the return value to the output field.

Input Field

Field	Offset (in Hex)	Length
Major Function Number	00	Byte
Minor Function Number	01	Byte
Parameter 1	02	Word
Parameter 2	04	Word
Parameter 3	06	Word
Parameter 4	08	Double word
Parameter 5	0C	Double word

Output Field

Field	Offset (in Hex)	Length
Return Code	00	Byte
Auxiliary Return Code	01	Byte
Parameter 1	02	Word
Parameter 2	04	Word
Parameter 3	06	Word
Parameter 4	08	Double word
Parameter 5	0C	Double word

Sample in Assembler Language

```
;
; Input Parameter Structure
;
SMB_INPARAM          STRUC
  @SMBIN_FUNC        DB      ?
  @SMBIN_SUB_FUNC    DB      ?
  @SMBIN_PARM_1      DW      ?
  @SMBIN_PARM_2      DW      ?
  @SMBIN_PARM_3      DW      ?
  @SMBIN_PARM_4      DD      ?
  @SMBIN_PARM_5      DD      ?
SMB_INPARAM          ENDS
```

```
;
; Output Parameter Structure
;
SMB_OUTPARAM        STRUC
  @SMBOUT_RC         DB      ?
  @SMBOUT_SUB_RC     DB      ?
  @SMBOUT_PARM_1     DW      ?
  @SMBOUT_PARM_2     DW      ?
  @SMBOUT_PARM_3     DW      ?
  @SMBOUT_PARM_4     DD      ?
  @SMBOUT_PARM_5     DD      ?
SMB_OUTPARAM        ENDS
```

Sample in C Language

```
//  
// Input Parameter Structure  
//  
typedef struct {  
    BYTE    SMBIN_FUNC    ;  
    BYTE    SMBIN_SUB_FUNC ;  
    WORD    SMBIN_PARM_1  ;  
    WORD    SMBIN_PARM_2  ;  
    WORD    SMBIN_PARM_3  ;  
    DWORD   SMBIN_PARM_4  ;  
    DWORD   SMBIN_PARM_5  ;  
} INPARAM, PINPARAM ;  
  
//  
// Output Parameter Structure  
//  
typedef struct {  
    BYTE    SMBOUT_RC      ;  
    BYTE    SMBOUT_SUB_RC ;  
    WORD    SMBOUT_PARM_1  ;  
    WORD    SMBOUT_PARM_2  ;  
    WORD    SMBOUT_PARM_3  ;  
    DWORD   SMBOUT_PARM_4  ;  
    DWORD   SMBOUT_PARM_5  ;  
} OUTPARAM, POUTPARAM ;  
  
typedef INPARAM    far    FPINPARAM ;  
typedef OUTPARAM   far    FPOUTPARAM ;
```

Calling Convention Pseudo Code

The following describes the calling convention using pseudo code.

Assembler Language

```
InputParm      SMB_INPARAM    < >  
OutputParm     SMB_OUTPARAM   < >
```

16-bit

```
    push    ds  
    mov     ax, offset OutputParm  
    push   ax  
    push   ds  
    mov     ax, offset InputParm  
    push   ax  
    call   dword ptr SmapiBios  
    add    sp, 8
```

32-bit

```
    push    ds  
    mov     eax, offset OutputParm  
    push   eax  
    push   ds  
    mov     eax, offset InputParm  
    push   eax  
    call   fword ptr SmapiBios  
    add    sp, 16
```

C Language

```
typedef WORD (far  SMB)(FPINPARAM, FOUTPARAM) ;  
  
SMB      SmapiBios ;  
INPARAM  InputParm ;  
OUTPARAM OutputParm ;  
WORD     RC ;  
  
RC = SmapiBios(&InputParm, &OutputParm) ;
```

Return Codes

The following hexadecimal return codes are stored in both the AL (AX) register and the return code field of the output parameter:

	No error
53	SMAPI function is not available
81	Invalid parameter
86	Function is not supported
9	System error
91	System is invalid
92	System is busy
A	Device error (disk read error)
A1	Device is busy
A2	Device is not attached
A3	Device is disabled
A4	Request parameter is out of range
A5	Request parameter is not accepted

All other values are reserved.

Function Description

System Information Service

Get System Identification

Input Field

Major Function Number -
Minor Function Number -
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Return value format
= - ASCII format
= 1 - Binary format
Parameter 1 - System ID
Parameter 2 - Country Code
Parameter 3 - System BIOS revision
Parameter 4 - (Bits 31-16) Reserved
- (Bits 15-) System Management BIOS revision
Parameter 5 - (Bits 31-16) Reserved
- (Bits 15-) SMI BIOS Interface revision

Get CPU Information

Input Field

Major Function Number -
Minor Function Number - 1
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - CPU ID
(Bits 15-8) Microprocessor type
(Bits 7-) Microprocessor stepping level
= FFFFh : Unknown
Parameter 3 - Clock Information
(Bits 15-8) CPU clock (units: MHz)
= FEh : CPU clock is over 254 MHz
= FFh : Unknown
(parameter 4 is valid)
(Bits 7-) Internal clock (units: MHz)
= FEh : Internal clock is over 254 MHz
= FFh : Unknown
(parameter 5 is valid)
Parameter 4 - (Bits 31-16) Reserved
- (Bits 15-) CPU clock (units : MHz)
Parameter 5 - (Bits 31-16) Reserved
- (Bits 15-) Internal clock (units: MHz)

Get Display Device Information

Input Field

Major Function Number -
Minor Function Number - 2
Parameter 1 - (Bit 8) LCD information
(Bit 9) External CRT information
(Bits 15-1) Reserved
(Bits 7-) Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - (Bits 15-8)
Built-in display device (panel)
information 1
= : Monochrome STN LCD
= 1 : Monochrome TFT LCD
= 2 : Color STN LCD
= 3 : Color TFT LCD
= FF : Unknown
(Bits 7-)
Built-in display device (panel)
information 2
= : 64 x48
= 1 : 8 x6
= 2 : 1 24x768
= FF : Unknown
Parameter 2 - (Bits 15-8) External CRT monitor
information
= : External CRT is not attached
= 1 : Color monitor
= 2 : Monochrome monitor
= FF : Unknown
(Bits 7-) Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Docking Station Information

Input Field

Major Function Number -
Minor Function Number - 3
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Docking station status
 Bit - Docking status
 = 0 : Undock
 = 1 : Dock
 Bits 5-1 - Reserved
 Bit 6 - Security key status
 = 0 : Lock position
 = 1 : Unlock position
 Bit 7 - Bus status
 = 0 : BUS isolated
 = 1 : BUS connected
Parameter 1 - Docking station ID
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get UltraBay II Information

Input Field

Major Function Number -
Minor Function Number - 4
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - (Bits 15-8) UltraBay device information
= : FDD
= 1 : Serial device
= 2 : TV tuner
= 1 : IDE device
= 2 : PCMCIA adapter
= 3 : Battery
= 4 : AC Adapter
= FE : No UltraBay
= FF : Unknown
(Bit 7-) UltraBay device ID
= : FDD
= 1 : Cellular
= 2 : TV tuner
= 1 : CD-ROM
= 11 : IDE-HDD
= 12 : DVD
= 13 : ZIP
= FF : ID is not available
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Slave Micro Control Unit Information

Input Field

Major Function Number -
Minor Function Number - 6
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Return value format
= - ASCII format
= 1 - Binary format
Parameter 1 - Reserved
Parameter 2 - Slave controller Revision
(= FFFF) - Not valid
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get System Sensor Status

Input Field

Major Function Number -
Minor Function Number - 7
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Current Status
 Bit 8 - LID Status
 = 0 : Open
 = 1 : Close
 Bit 9 - Keyboard status
 = 0 : Close
 = 1 : Open
 Bit 1 - AC Adapter
 = 0 : Not attached
 = 1 : Attached
 Bits 15-11 : Reserved
 Bits 7- : Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Video Information

Input Field

Major Function Number -
Minor Function Number - 8
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Video BIOS revision
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Refresh Rate Capability

Input Field

Major Function Number -
Minor Function Number - 9
Parameter 1 - mode
= xxh - VGA modes
(Bits -7 are ignored)
= 1 - 64 x4 x256
= 1 1 - 64 x48 x256
= 1 2 - 8 x6 x16
= 1 3 - 8 x6 x256
= 1 4 - 1 24x768x16
= 1 5 - 1 24x768x256
= 1 6 - 128 x1 24x16
= 1 7 - 128 x1 24x256
= 1 9 - 1 56x35 x16
= 1 A - 1 56x473x16
= 1 C - 1 56x48 x16
= 11 - 64 x48 x32K
= 111 - 64 x48 x64K
= 112 - 64 x48 x16M
= 113 - 8 x6 x32K
= 114 - 8 x6 x64K
= 115 - 8 x6 x16M
= 116 - 1 24x768x32K
= 117 - 1 24x768x64K
= 118 - 1 24x768x16M
= 119 - 128 x1 24x32K
= 11A - 128 x1 24x64K
= 11B - 128 x1 24x16M
= A - 16 x12 x16
= A 1 - 16 x12 x256
= A 2 - 16 x12 x32K
= A 3 - 16 x12 x64K
= A 4 - 16 x12 x16M
= Others : Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Refresh rate capability for
 specified mode:
 Bit - 6 Hz available
 Bit 1 - 72Hz available
 Bit 2 - 75Hz available
 Bit 3 - 43Hz(I) available
 Bit 4 - 56Hz available
 Bit 5 - 7 Hz available
 Bit 6 - 85Hz available
 Bit 7 - 48Hz(I) available
 Bits 8-15 : Reserved (must be B' ')
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

System Configuration Service

Get Display Device State

Input Field

Major Function Number - 1

Minor Function Number -

Parameter 1 - Request type
= h : Current hardware
= 1h : CMOS
(effective after reboot)

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Bits 15-8 : Reserved
Bits 7- : Capability of display device function
Bit - Display function type
= : Not support
= 1 : Support
Bits 7-1 : Reserved
Parameter 2 - Bits 15-8 Display current status
Bit - Built-in display (panel) status
= : Disable
= 1 : Enable
Bit 1 - External CRT status
= : Disable
= 1 : Enable
Bit 2 - TV status
= : Disable
= 1 : Enable
Bits 6-3 : Reserved
Bit 7 - Dual enable flag
= : Disable
= 1 : Enable
Bits 7- : Display function type
= h : No TV-out model
= 1h : Not support model for simultaneous display of TV and CRT
Parameter 3 - Reserved
Parameter 4 - When parameter 2 (bits 7-) is 1h:
Bits 31-16 : Reserved
Bits 15- : Display selection mode
Bit - Display selection mode
= : LCD - CRT selection mode
= 1 : LCD - TV selection mode
Bits 7-1 : Reserved
Parameter 5 - Reserved

Set Display Device State

Input Field

Major Function Number - 1
Minor Function Number - 1
Parameter 1 - Request display status
Bit - Built-in display (panel) status
= : Disable
= 1 : Enable
Bit 1 - External CRT status
= : Disable
= 1 : Enable
Bit 2 - TV status
= : Disable
= 1 : Enable
Bits 5-3 : Reserved
Bit 6 - Monitor detection ignore
= : Do not ignore
= 1 : Ignore
Bit 7 - Dual enable flag
= : Disable
= 1 : Enable
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - When parameter 2 (bits 7-) is 1h in return
of "Get Display Device State":
Bits 31-16 : Reserved
Bits 15- : Display selection mode
Bit - Display selection mode
= : LCD - CRT selection mode
= 1 : LCD - TV selection mode
Bits 7-1 : Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Pointing Device State

Input Field

Major Function Number - 11
Minor Function Number - 2
Parameter 1 - Bits 15-8 Request type
= h - Current hardware
= 1h - CMOS (effective after reboot)
Bits 7- Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Bits 15-8 Pointing device current status
Bits 1 , 8 - Built-in pointing device control
= : Disable
= 1 : Enable
= 1 : Auto
= 11 : Reserved
Bit 9 - External pointing device status
= : Disable
= 1 : Enable
Bits 15-11: Reserved
Bits 7- Pointing device capability
Bit - Built-in pointing device status
= : Status is not controllable
= 1 : Status is controllable
Bit 1 - External pointing device status
= : Status is not controllable
= 1 : Status is controllable
Bit 2 - Built-in pointing device auto control
= : Not support
= 1 : Support
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Set Pointing Device State

Input Field

Major Function Number - 11
Minor Function Number - 3
Parameter 1 - Reserved
Parameter 2 - Bits 15-8
Pointing device current status
Bits 1 , 8 - Built-in pointing device
auto control
= : Disable
= 1 : Enable
= 1 : Auto
= 11 : Reserved
Bit 9 - External pointing device status
= : Disable
= 1 : Enable
Bits 15-11: Reserved
Bits 7- Request type
= h - Current hardware
= 1h - CMOS (effective after reboot)
Bits 7-2: Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Hotkey Sticky/Lock

Input Field

Major Function Number - 13
Minor Function Number - 2
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Bits 15-8 Capability
Bit 8 - Sticky Fn key support
Bit 9 - Sticky & Lock Fn key support
Bits 15-1 - Reserved
Bits 7- Current status
= : Disable
= 1 : Sticky Fn key
= 3 : Sticky & Lock Fn key
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Set Hotkey Sticky/Lock

Input Field

Major Function Number - 13
Minor Function Number - 3
Parameter 1 - Bits 15-8 Reserved
Bits 7- Request Status
= : Disable
= 1 : Sticky Fn key
= 3 : Sticky & Lock Fn key
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Power Management Service

Get Power Management Mode

Input Field

Major Function Number - 22
Minor Function Number -
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Bits 15-8 Power management mode
 Battery operation
 = h - High performance mode
 = 1h - Auto power management mode
 = 2h - Manual power management mode
Bits 7- Power management mode
 ac operation
 = h - High performance mode
 = 1h - Auto power management mode
 = 2h - Manual power management mode
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Set Power Management Mode

Input Field

Major Function Number - 22

Minor Function Number - 1

Parameter 1 - Bits 15-8 Power management mode
Battery operation
= h - High performance mode
= 1h - Auto power management mode
= 2h - Manual power management mode
Bits 7- Power management mode
ac operation
= h - High performance mode
= 1h - Auto power management mode
= 2h - Manual power management mode

Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Reserved

Parameter 2 - Reserved

Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Get Timer Control

Input Field

Major Function Number - 22

Minor Function Number - 2

Parameter 1 - Reserved

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Bits 15-8 Capability of timer control
Bit 8 - System
(Hibernation/suspend) timer
= 0 : Not support
= 1 : Support
Bit 9 - Standby timer
= 0 : Not support
= 1 : Support
Bit 10 - LCD off timer
= 0 : Not support
= 1 : Support
Bit 11 - HDD off timer
= 0 : Not support
= 1 : Support
Bits 15-12 - Reserved
Bits 7-4 - Timer control
Bit 7 - System (Hibernation/suspend)
timer
= 0 : Disable
= 1 : Enable
Bit 6 - Standby timer
= 0 : Disable
= 1 : Enable
Bit 5 - LCD off timer
= 0 : Disable
= 1 : Enable
Bit 4 - HDD off timer
= 0 : Disable
= 1 : Enable
Bits 7-4 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Set Timer Control

Input Field

Major Function Number - 22
Minor Function Number - 3
Parameter 1 - Bits 15-8 Reserved
Bits 7- Timer control
Bit - System
(Hibernation/suspend) timer
= : Disable
= 1 : Enable
Bit 1 - Standby timer
= : Disable
= 1 : Enable
Bit 2 - LCD off timer
= : Disable
= 1 : Enable
Bit 3 - HDD off timer
= : Disable
= 1 : Enable
Bits 7-4 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Event Bit Definition

Bits 2- - Reserved
Bit 3 - Standby
Bit 4 - Suspend
Bit 5 - RediSafe
Bit 6 - Hibernation
Bit 7 - Power off

Note: If bits are duplicated, the highest bit is available.

Get System Event Global Condition

Input Field

Major Function Number - 3
Minor Function Number -
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Bits 15-8 Capability for event
 Bit 8 - RediSafe is
 controlled by global conditions.
 (The RediSafe bit is ignored
 in each event condition.)
 = - Not support
 = 1 - Support
Bits 7- Global event condition
 Bit - Enable RediSafe
 if suspend is selected.
 = - Disable
 = 1 - Enable
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Set System Event Global Condition

Input Field

Major Function Number - 3
Minor Function Number - 1
Parameter 1 - Bits 15-8 Reserved
Bits 7- Global condition for event
Bit - Enable safe suspend if suspend
is selected.
= - Disable
= 1 - Enable
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get System Event 1 Condition

Input Field

Major Function Number - 31
Minor Function Number -
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Hardware and software event definition
Bits 15-8 - Capability (see page B-34)
Bits 7- - Condition (see page B-34)
Parameter 3 - Reserved
Parameter 4 - Bits 31-16 : Reserved
Bits 15- Power switch detection event definition
Bits 15-8 - Capability (see page B-34)
Bits 7- - Condition (See page B-34)
Parameter 5 - Bits 31-16 : Reserved
Bits 15- LID close detection event definition
Bits 15-8 - Capability (see page B-34)
Bits 7- - Condition (see page B-34)

Set System Event 1 Condition

Input Field

Major Function Number - 31
Minor Function Number - 1
Parameter 1 - Condition for hardware and software event
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Bits 31-16 : Reserved
Bits 15- Condition for power
switch detection
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)
Parameter 5 - Bits 31-16 : Reserved
Bits 15- Condition for
LID close detection
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get System Event 2 Condition

Input Field

Major Function Number - 32

Minor Function Number -

Parameter 1 - System timer expiration event definition
Bits 15-8 - Capability (see page B-34)
Bits 7- - Condition (see page B-34)

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Bits 31-16 : Reserved
Bits 15- Standby timer expiration event definition
Bits 15-8 - Capability (see page B-34)
Bits 7- - Condition (see page B-34)

Parameter 5 - Bits 31-16 : Reserved
Bits 15- Hibernation timer during suspend mode expiration event definition.
Bits 15-8 - Capability (see page B-34)
Bits 7- - Condition (see page B-34)

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Reserved

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Set System Event 2 Condition

Input Field

Major Function Number - 32

Minor Function Number - 1

Parameter 1 - Condition for system timer expiration
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Bits 31-16 : Reserved
Bits 15- Condition for standby
timer expired
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)

Parameter 5 - Bits 31-16 : Reserved
Bits 15- Condition for hibernation
timer during suspend mode expired
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Reserved

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Get System Timer

Input Field

Major Function Number - 32

Minor Function Number - 2

Parameter 1 - Bits 15-8 Power mode select
= h - Reserved
= 1h - Manual PM mode (ac)
= 2h - Manual PM mode (battery)
= F3h - High performance mode
= F4h - Auto power management mode
Bits 7- Reserved

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Bits 15-8 System timer capability
Bit 8 = - Timer cannot be specified
in each power mode
= 1 - Timer can be specified
in each Power mode
Bits 15-9 : Reserved
Bits 7- : Reserved

Parameter 2 - Bits 15-8 : Reserved
Bits 7- System timer initial value
(units: minutes)
= h - Disable system timer

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Set System Timer

Input Field

Major Function Number - 32

Minor Function Number - 3

Parameter 1 - Bits 15-8 Power mode select
= h - All mode
= 1h - Manual PM mode (AC)
= 2h - Manual PM mode (battery)
= F3h - High performance mode
= F4h - Auto power management mode
Bits 7- System timer initial
value (units: minutes)
= h - Disable system timer

Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get Hibernation Timer

Input Field

Major Function Number - 32
Minor Function Number - 6
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Bits 15-8 : Reserved
Bits 7- Hibernation timer during
suspend mode initial value
(units: minutes)
= h - Disable hibernation timer
during suspend mode
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Set Hibernation Timer

Input Field

Major Function Number - 32

Minor Function Number - 7

Parameter 1 - Bits 15-8 : Reserved
Bits 7- Hibernation timer during
suspend mode initial value
(units: minutes)
= h - Disable hibernation timer
during suspend mode

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Reserved

Parameter 2 - Reserved

Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Get System Event 3 Condition

Input Field

Major Function Number - 33
Minor Function Number -
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Critical low battery condition
detection event definition
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)
Parameter 3 - Reserved
Parameter 4 - Bits 16-31 : Reserved
Bits -15 Out-of-environment condition
detection event definition
Bits 15-8 - Capability
(see page B-34)
Bits 7- - Condition
(see page B-34)
Parameter 5 - Reserved

Set System Event 3 Condition

Input Field

Major Function Number - 33

Minor Function Number - 1

Parameter 1 - Bits 15-8 : Reserved
Bits 7- Condition for critical
low battery condition detection
Bits 7- - Condition
(see page B-34)

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Bits 31-8 : Reserved
Bits 7- Condition for out-of-environment
condition detection
Bits 7- - Condition
(see page B-34)

Parameter 5 - Reserved

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Reserved

Parameter 2 - Reserved

Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Get System Resume Condition

Input Field

Major Function Number - 34

Minor Function Number -

Parameter 1 - Reserved

Parameter 2 - Reserved

Parameter 3 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Output Field

Return Code - Error status

Auxiliary Return Code - Reserved

Parameter 1 - Reserved

Parameter 2 - Condition for resuming trigger from system suspend mode

Bit - Resume switch by hardware

Bit 1 - LID open detection

Bit 2 - RTC alarm (resume timer) detection

Bit 3 - RI from the serial device detection

Bits 15-4 - Reserved

Parameter 3 - Capability for resuming trigger from the system suspend mode

Bit - Resume switch by hardware

Bit 1 - LID open detection

Bit 2 - RTC alarm (resume timer) detection

Bit 3 - RI from the serial device detection

Bits 15-4 - Reserved

Parameter 4 - Reserved

Parameter 5 - Reserved

Set System Resume Condition

Input Field

Major Function Number - 34

Minor Function Number - 1

Parameter 1 - Condition for resuming trigger from the system suspend mode
Bit - Resume switch by hardware
Bit 1 - LID open detection
Bit 2 - RTC alarm (resume timer) detection
Bit 3 - RI from the serial device detection
Bits 15-4 : Reserved

Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Get System Resume Timer

Input Field

Major Function Number - 34
Minor Function Number - 2
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - TOD of resume timer (BCD format)
Bits 7- - Seconds (-59)
Bits 15-8 - Minutes (-59)
Bits 23-16 - Hours (-23)
Bits 31-24 - Reserved
Parameter 5 - Date of resume timer (BCD format)
Bits 7- - Day (1-31)
Bits 15-8 - Month (1-12)
Bits 23-16 - Year (-99)
Bits 3 -24 - Reserved
Bit 31 - Resume date validation
= - Valid (specified day)
= 1 - Invalid (every day)

Set System Resume Timer

Input Field

Major Function Number - 34
Minor Function Number - 3
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - TOD of resume timer (BCD format)
Bits 7- - Seconds (-59)
Bits 15-8 - Minutes (-59)
Bits 23-16 - Hours (-23)
Bits 31-24 - Reserved
Parameter 5 - Date of resume timer (BCD format)
Bits 7- - Day (1-31)
Bits 15-8 - Month (1-12)
Bits 23-16 - Year (-99)
Bits 3 -24 - Reserved
Bit 31 - Resume date validation
= - Valid (specified day)
= 1 - Invalid (every day)

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Request System Standby

Input Field

Major Function Number - 7
Minor Function Number -
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Request System Suspend

Input Field

Major Function Number - 7
Minor Function Number - 1
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Request System Hibernation

Input Field

Major Function Number - 7
Minor Function Number - 2
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Request System Off

Input Field

Major Function Number - 7
Minor Function Number - 3
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Output Field

Return Code - Error status
Auxiliary Return Code - Reserved
Parameter 1 - Reserved
Parameter 2 - Reserved
Parameter 3 - Reserved
Parameter 4 - Reserved
Parameter 5 - Reserved

Samples

Data Structure

Assembler Language

```
;
; SMAPI BIOS Header
;
SMB_HEADER          STRUC
@SMBHDR_SIG         DB  4 dup (?) ; + - Signature
@SMBHDR_VER         DB  ?          ; + 4 - Major version
@SMBHDR_VER_VER     DB  ?          ; + 5 - Minor version
@SMBHDR_LEN         DB  ?          ; + 6 - Length
@SMBHDR_CHKSUM      DB  ?          ; + 7 - Checksum
@SMBHDR_INFO        DW  ?          ; + 8 - Information word
@SMBHDR_RSV1        DW  ?          ; + A - Reserve 1
@SMBHDR_R_OFFSET    DW  ?          ; + C - Real mode offset
@SMBHDR_R_SEGMENT   DW  ?          ; + E - Real mode segment
@SMBHDR_RSV2        DW  ?          ; +1 - Reserve 2
@SMBHDR_P16_OFFSET  DW  ?          ; +12 - 16-bit protected mode offset
@SMBHDR_P16_BASE    DD  ?          ; +14 - 16-bit protected mode base address
@SMBHDR_P32_OFFSET  DD  ?          ; +18 - 32-bit protected mode offset
@SMBHDR_P32_BASE    DD  ?          ; +1C - 32-bit protected mode base address
SMB_HEADER          ENDS
```

Parameters

```
;
;Input Parameter
;
SMB_INPARAM          STRUC
@SMBIN_FUNC          DB      ?
@SMBIN_SUB_FUNC      DB      ?
@SMBIN_PARM_1        DW      ?
@SMBIN_PARM_2        DW      ?
@SMBIN_PARM_3        DW      ?
@SMBIN_PARM_4        DD      ?
@SMBIN_PARM_5        DD      ?
SMB_INPARAM          ENDS

;
;Output Parameter
;
SMB_OUTPARAM         STRUC
@SMBOUT_RC           DB      ?
@SMBOUT_SUB_RC       DB      ?
@SMBOUT_PARM_1       DW      ?
@SMBOUT_PARM_2       DW      ?
@SMBOUT_PARM_3       DW      ?
@SMBOUT_PARM_4       DD      ?
@SMBOUT_PARM_5       DD      ?
SMB_OUTPARAM         ENDS
```

C Language

```
//  
// SMAPI BIOS Header  
//  
typedef struct {  
    BYTE    SMBHDR_SIG[4]      ; // Signature  
    BYTE    SMBHDR_VER        ; // Major version  
    BYTE    SMBHDR_VER_VER    ; // Minor version  
    BYTE    SMBHDR_LEN        ; // Length  
    BYTE    SMBHDR_CHKSUM     ; // Checksum  
    WORD    SMBHDR_INFO       ; // Information word  
    WORD    SMBHDR_RSV1       ; // Reserve 1  
    WORD    SMBHDR_R_OFFSET   ; // Real mode offset  
    WORD    SMBHDR_R_SEGMENT  ; // Real mode segment  
    WORD    SMBHDR_RSV2       ; // Reserve 2  
    WORD    SMBHDR_P16_OFFSET ; // 16-bit Protect mode offset  
    DWORD   SMBHDR_P16_BASE   ; // 16-bit Protect mode base address  
    DWORD   SMBHDR_P32_OFFSET ; // 32-bit Protect mode offset  
    DWORD   SMBHDR_P32_BASE   ; // 32-bit Protect mode base address  
} SMB_HEADER, PSMB_HEADER ;
```

Parameters

```
//
// Input Parameter
//
typedef struct {
    BYTE    SMBIN_FUNC        ;
    BYTE    SMBIN_SUB_FUNC   ;
    WORD    SMBIN_PARM_1     ;
    WORD    SMBIN_PARM_2     ;
    WORD    SMBIN_PARM_3     ;
    DWORD   SMBIN_PARM_4     ;
    DWORD   SMBIN_PARM_5     ;
} INPARAM, PINPARAM ;

//
// Output Parameter
//
typedef struct {
    BYTE    SMBOUT_RC        ;
    BYTE    SMBOUT_SUB_RC   ;
    WORD    SMBOUT_PARM_1    ;
    WORD    SMBOUT_PARM_2    ;
    WORD    SMBOUT_PARM_3    ;
    DWORD   SMBOUT_PARM_4    ;
    DWORD   SMBOUT_PARM_5    ;
} OUTPARAM, POUTPARAM ;

typedef INPARAM far    FPINPARAM;
typedef OUTPARAM far   FPOUTPARAM;
```

Function Declaration

C Language

```
//  
// SMAPI BIOS function  
//  
typedef WORD (far  SMB)(FPINPARAM, FPOUTPARAM) ;
```

Installation Check

Assembler Language: Real Mode

```
;
; FindSmapi
; -----
;
; On Entry : None
; On Exit  : CF = .. Find out
;           DX - Segment
;           BX - Pointer to header
;
;           CF = 1 .. No SMAPI BIOS
;

FindSmapi      Proc    Near

    push    eax
    push    cx
    push    si
    push    ds

    mov     ax, BIOS_SEG      ; F    Segment
    mov     ds, ax
    mov     bx,              ; Start point
    mov     cx, SMB_CAND_CNT ; Total check count
    mov     eax, 'BMS$'     ; Target strings

@@:
    cmp     eax, dword ptr ds:[bx].@SMBHDR_SIG
    je     short @f
    add     bx, 1 h         ; Next paragraph
    loop   @b
    stc
    jmp     short FindSmapiFin
```

```

@@: ; Find Smapi Head
    mov     dx, BIOS_SEG

    ; Calculate Checksum.. next.
    pushf                    ; Save direction flag
    cld                      ; Clear it
    mov     si, bx
    xor     ax, ax
    movzx   cx, byte ptr ds:[bx].@SMBHDR_LEN
@@:
    lodsb
    add     ah, al
    loop   @b

    popf                    ; Restore Direction flags
    cmp     ah, 1           ; Checksum is OK?
    cmc

FindSmapiFin:
    pop     ds
    pop     si
    pop     cx
    pop     eax
    ret

FindSmapi      Endp

```


C Language

```
typedef struct {
    BYTE    SMBHDR_SIG[4]        ; // Signature
    BYTE    SMBHDR_VER           ; // Major version
    BYTE    SMBHDR_VER_VER      ; // Minor version
    BYTE    SMBHDR_LEN          ; // Length
    BYTE    SMBHDR_CHKSUM       ; // Checksum
    WORD    SMBHDR_INFO         ; // Information word
    WORD    SMBHDR_RSV1         ; // Reserve 1
    WORD    SMBHDR_R_OFFSET     ; // Real mode offset
    WORD    SMBHDR_R_SEGMENT    ; // Real mode segment
} SMB_HEADER_REAL, far  PFSMB_HEADER_REAL ;
```

```

BOOLEAN GetSmapiEntry(PSMB pFunc)
{
    PFSMB_HEADER_REAL    MyPtr = xF          ;
    WORD                 cnt =          ;
    BYTE                 cksum =          ;

    //
    // 1) Search for signature first
    //
    while((cnt++ < x1    ) &&
          !(((MyPtr->SMBHDR_SIG)[ ] == '$') &&
            ((MyPtr->SMBHDR_SIG)[1] == 'S') &&
            ((MyPtr->SMBHDR_SIG)[2] == 'M') &&
            ((MyPtr->SMBHDR_SIG)[3] == 'B') )) {
        MyPtr++ ;
    }

    //
    // 2) Find the Signature?
    //
    if (cnt >= x1    ) {
        // We cannot find it.
        return FALSE ;
    } else {
        //
        // 3) Calculate Checksum
        //
        for (cnt =          ; cnt < MyPtr->SMBHDR_LEN ; cnt++)
            cksum += (BYTE)((MyPtr->SMBHDR_SIG)[cnt]) ;

        if (cksum) {
            // Bad Checksum
            return FALSE ;
        } else {
            // Build Return Address
            ( pFunc ) = ( (DWORD)(MyPtr->SMBHDR_R_OFFSET) +
                          (((DWORD)(MyPtr->SMBHDR_R_SEGMENT)) << 16) ) ;
            return TRUE ;
        }
    }
}

```

BIOS Call

Assembler Language: 16-Bit Protected Mode

```
;  
; Build Input Parameter Field  
;  
  
mov     al, SMB_GET_SYSID  
mov     [bx].@Func, al  
  
push    ds  
mov     ax, offset OutputParm  
push    ax  
push    ds  
  
mov     ax, offset InputParm  
push    ax  
call    _SmapiBios  
add     sp, 8  
  
;  
; Get information from Output Parm  
;  
or      ax, ax  
jnz     Error  
  
mov     bx, offset OutputParm  
mov     al, [bx].@Parm1
```

32-Bit Protected Mode

```
;
; Build Input Parameter Field
;
mov     ebx, offset InputParm
mov     al, SMB_GET_SYSID
mov     [ebx].@Func, al

push   ds
mov     eax, offset OutputParm
push   eax
push   ds
mov     eax, offset InputParm
push   eax
call   _SmapiBios
add    sp, 16

;
; Get information from Output Parm
;
or     ax, ax
jnz    Error

mov     ebx, offset OutputParm
mov     ax, [ebx].@Parm1
```

C Language

```
WORD GetSystemID()
{
    SMB          SmapiEntry ;
    INPARAM      MyInput ;
    OUTPARAM     MyOutput ;
    WORD         Rc = -1 ;

    if (GetSmapiEntry(&SmapiEntry)) {

        MyInput.SMBIN_FUNC      = ;
        MyInput.SMBIN_SUB_FUNC  = ;

        if (SmapiEntry(&MyInput, &MyOutput)) {
            // No System ID is available
        } else {
            Rc = MyOutput.SMBOUT_PARM_1 ;
        }

    } else {
        // No SMAPI BIOS interface.
        // Try to use CBIOS INT 15.
    }
    return Rc ;
}
```

Appendix C. Appendix C

:subject=Notices.

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